# Persistent Owicki-Gries Reasoning (POG)

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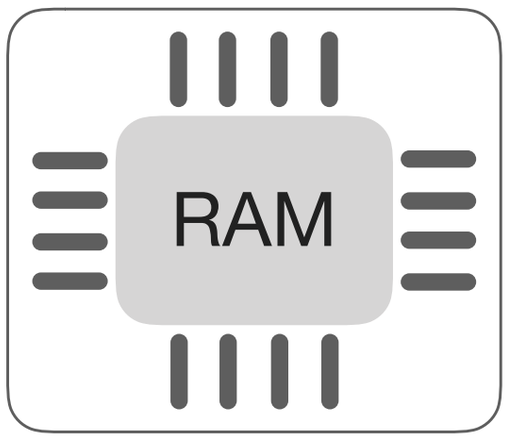
# Computer Storage

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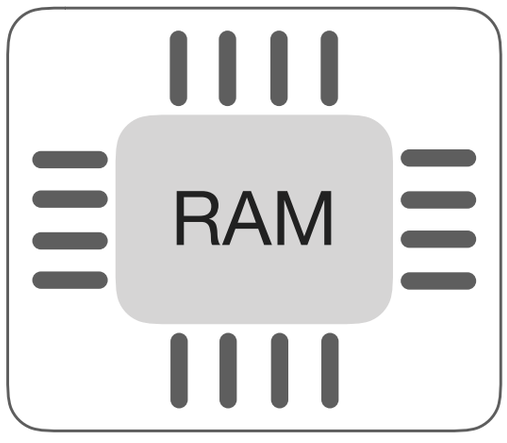
✗ *volatile*

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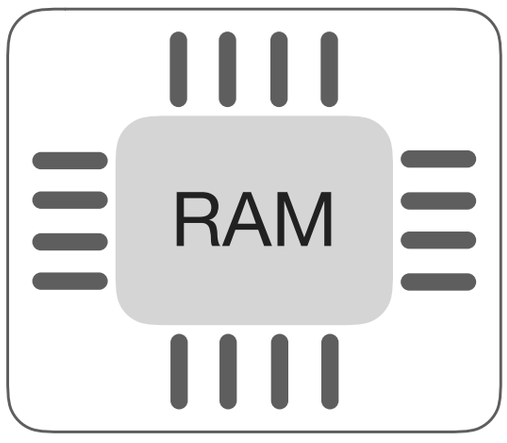
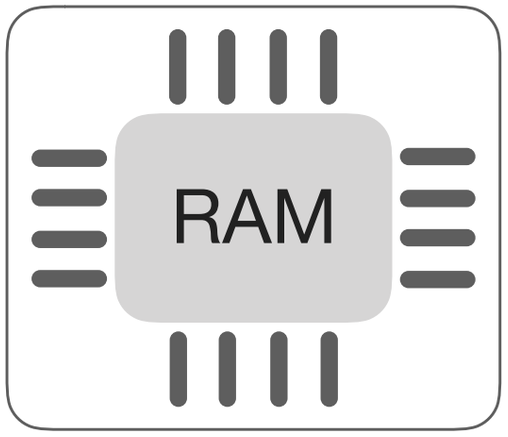




✗ *slow*
✓ *persistent*

# What is Non-Volatile Memory (NVM)?

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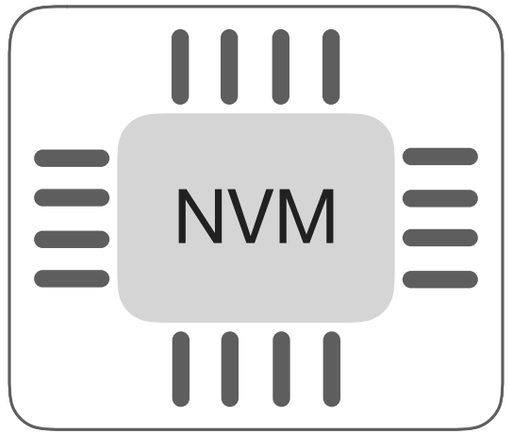


***NVM: Hybrid Storage + Memory***

Best of both worlds:

✓ ***persistent*** (like HDD)
✓ ***fast***, ***random access*** (like RAM)

# Formal Persistency (Low-Level) ***Semantics***

Intel® Architecture Reference Manual


⇓

The ***Px86*** Model

[Raad et al., POPL'20]

# x86: (Volatile) Concurrent Hardware Model (TSO)

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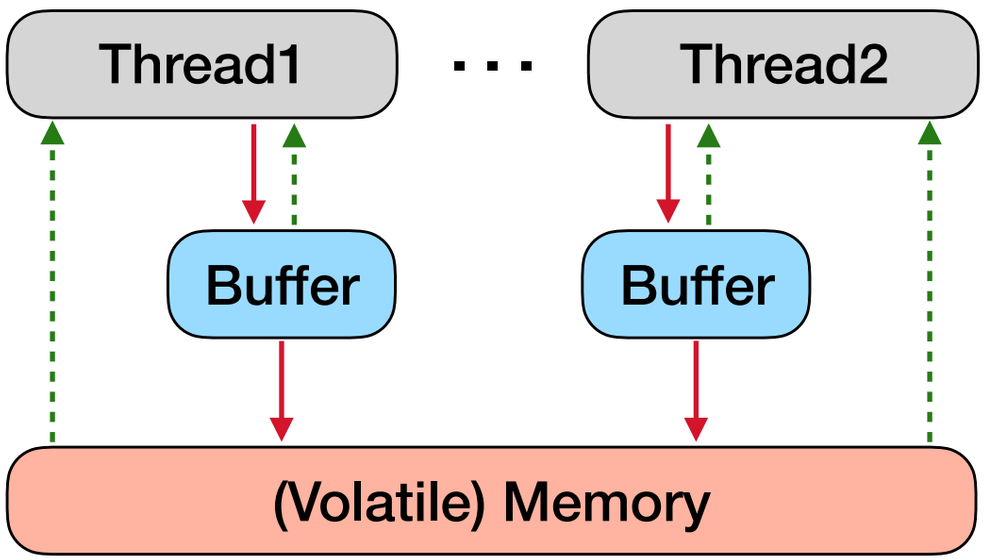

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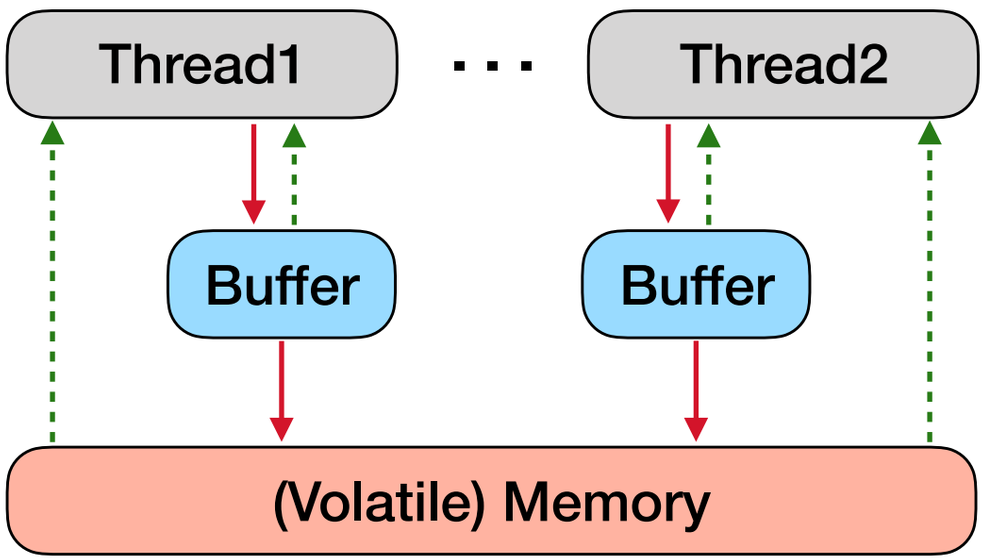


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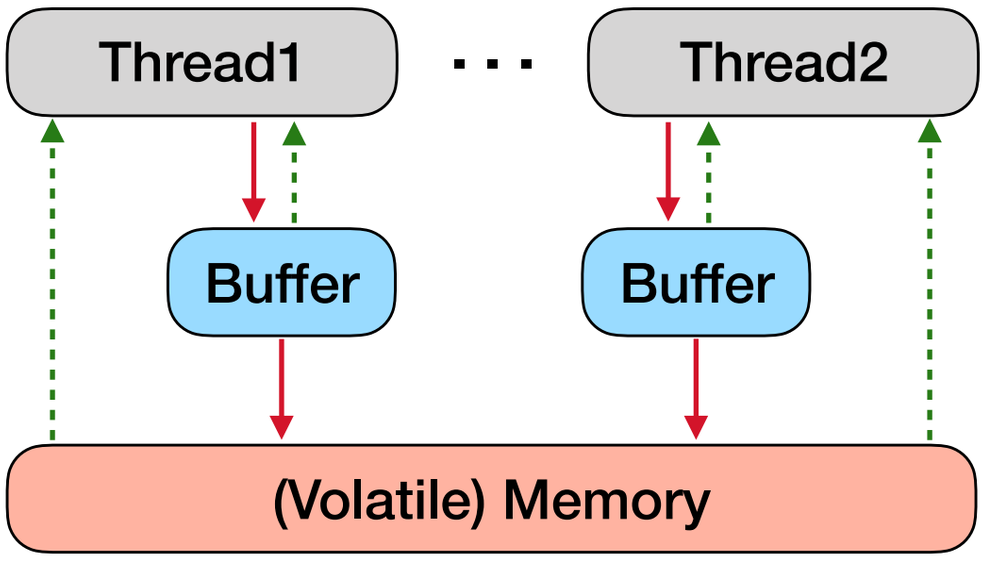


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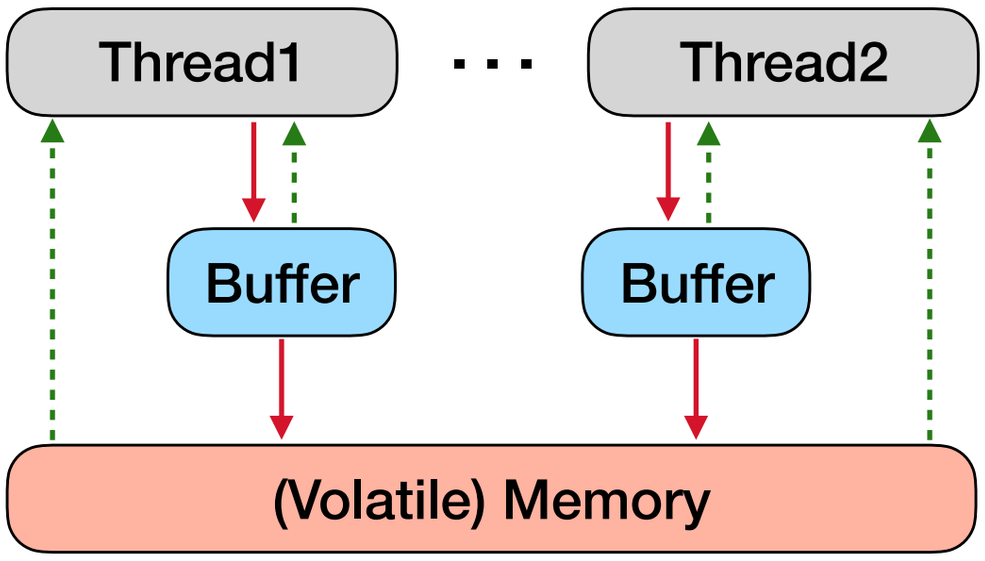


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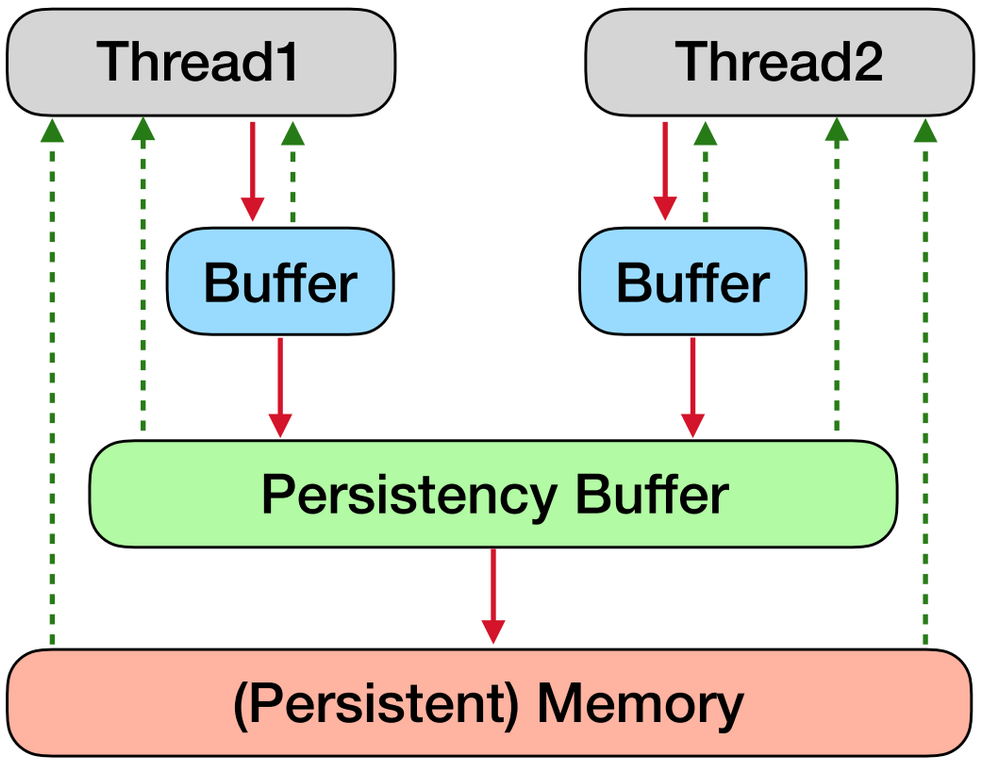


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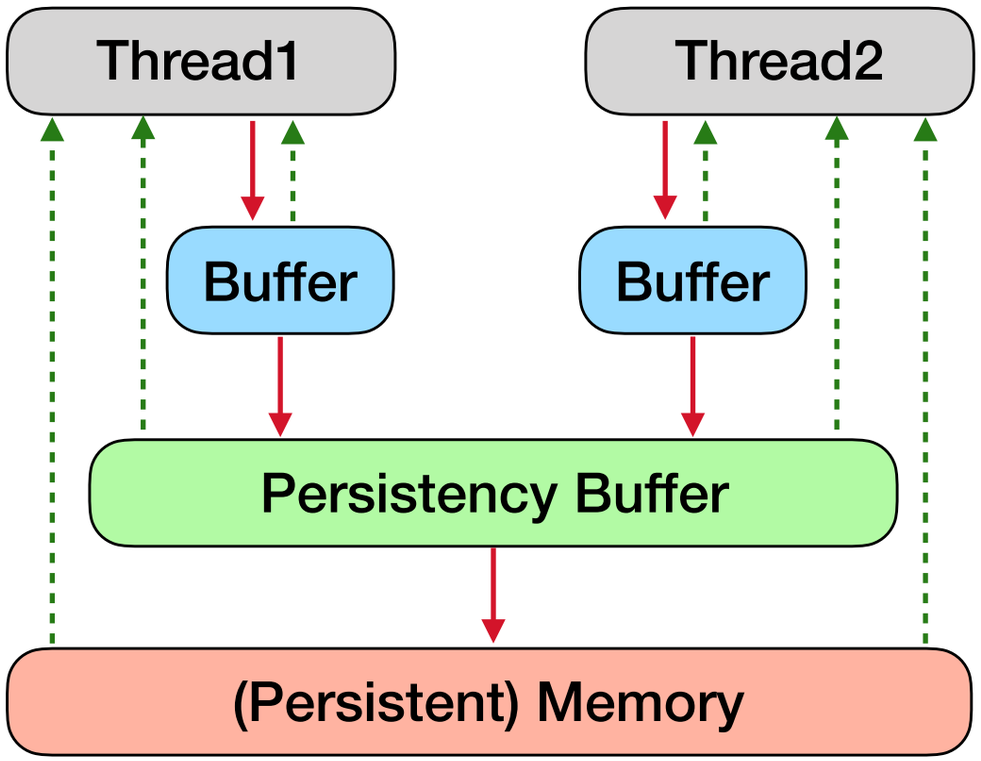


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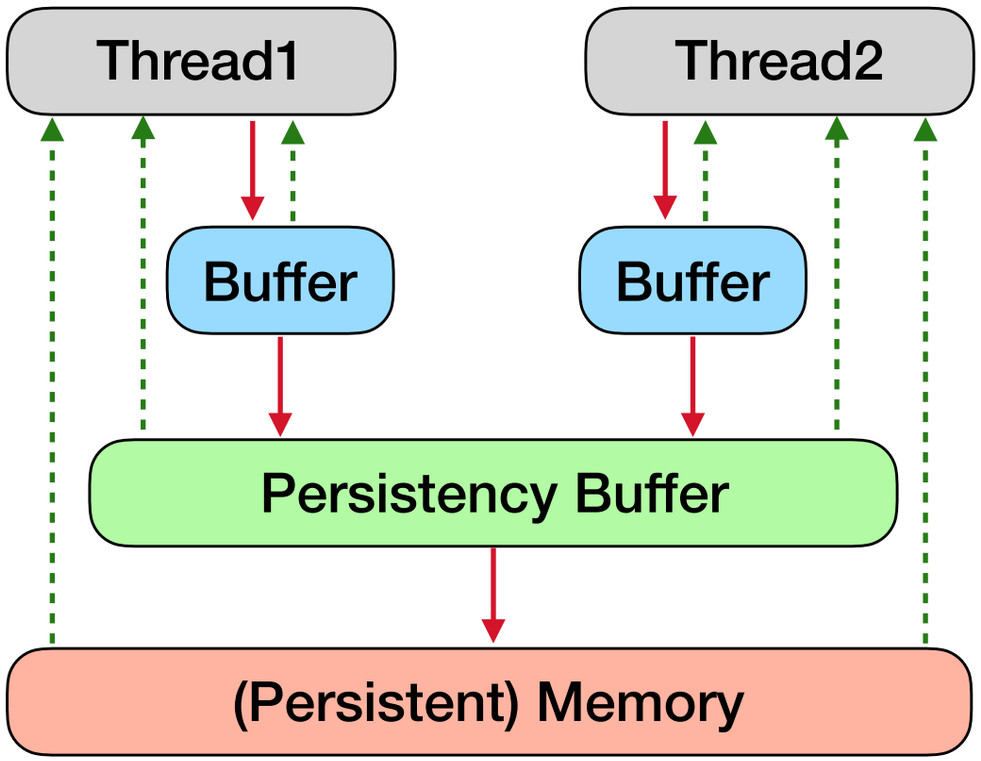


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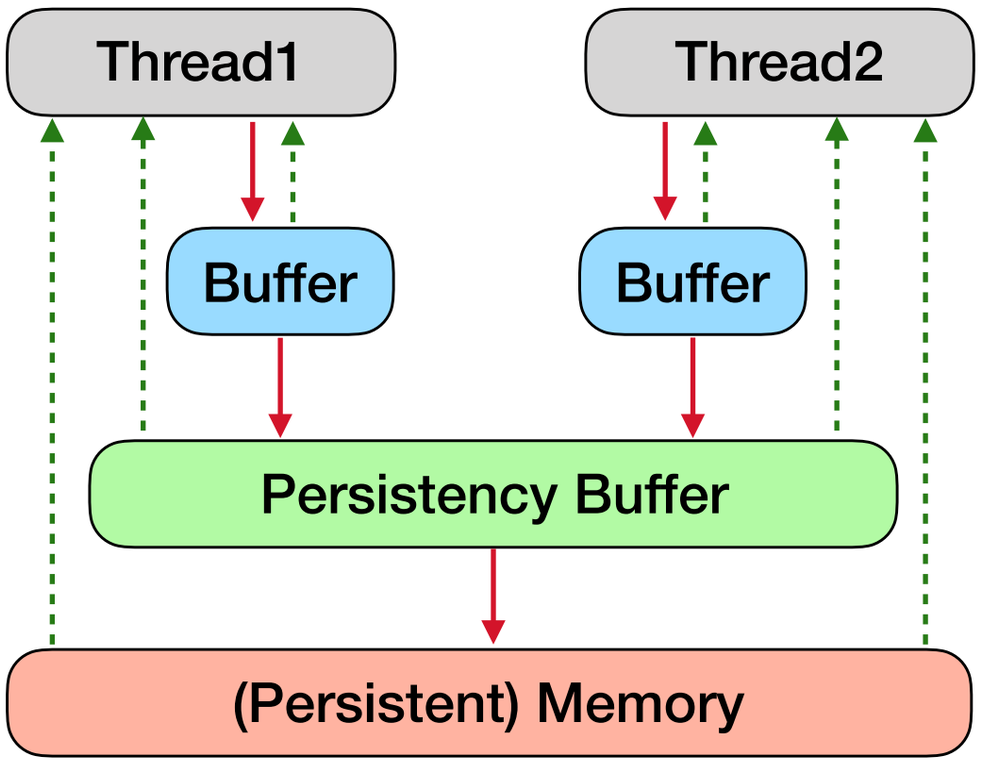


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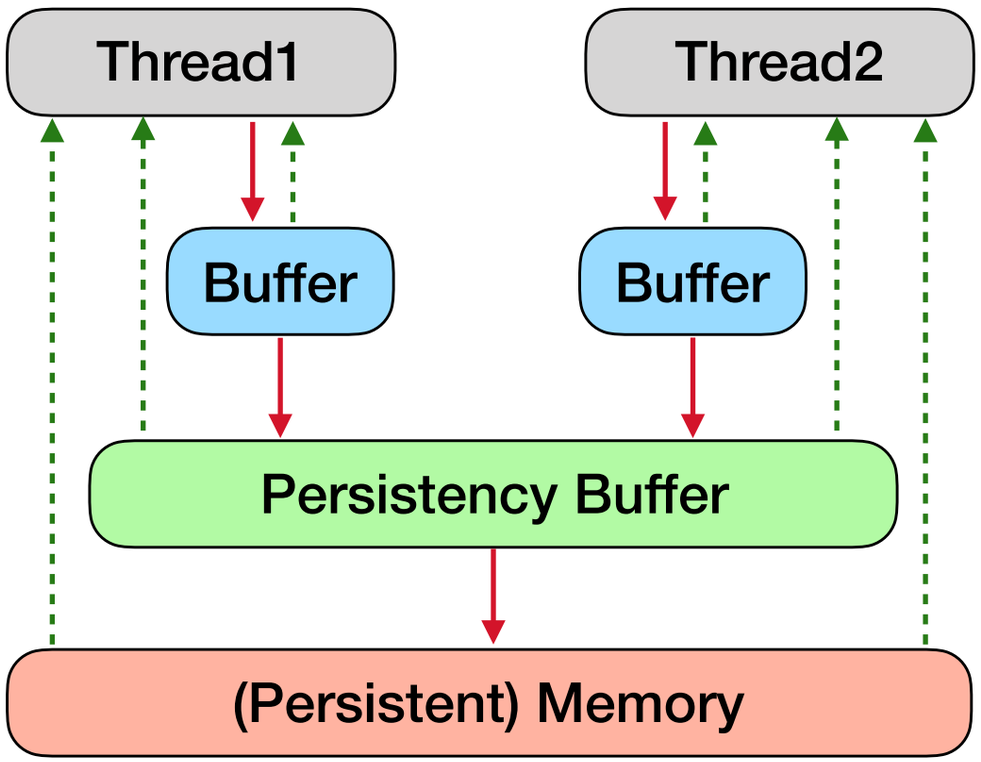


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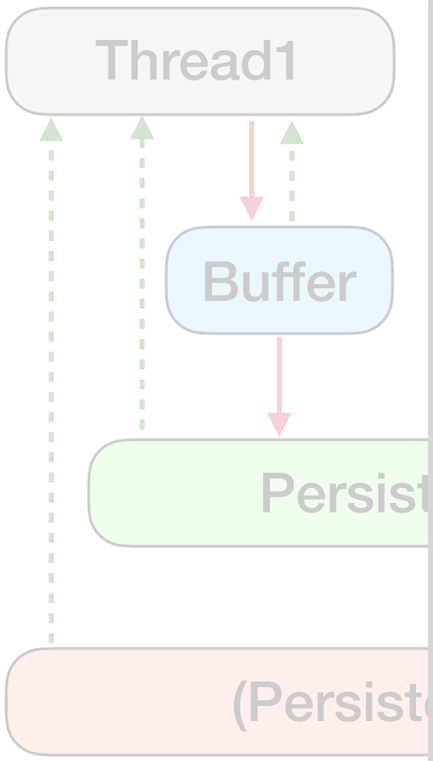


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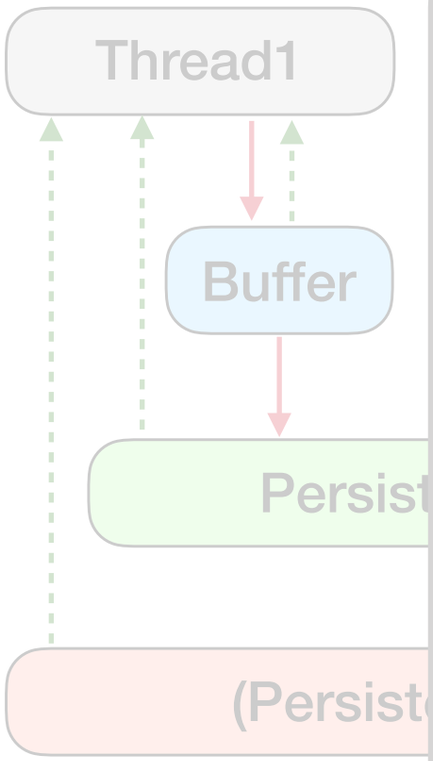


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## ***Solution***

- **high-level** reasoning via **program logics**
- reasoning over program **syntax**
- simpler to verify high-level invariants

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**Our Approach**

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  - ➡ ***translation*** from Px86 to lx86
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← **This talk**

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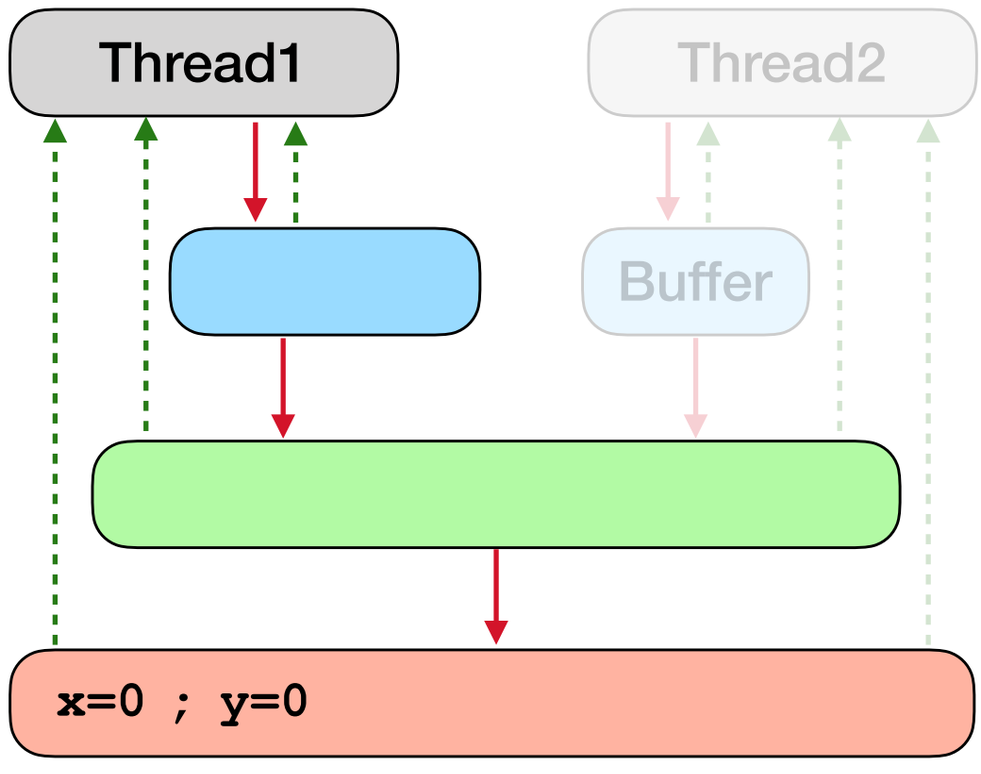

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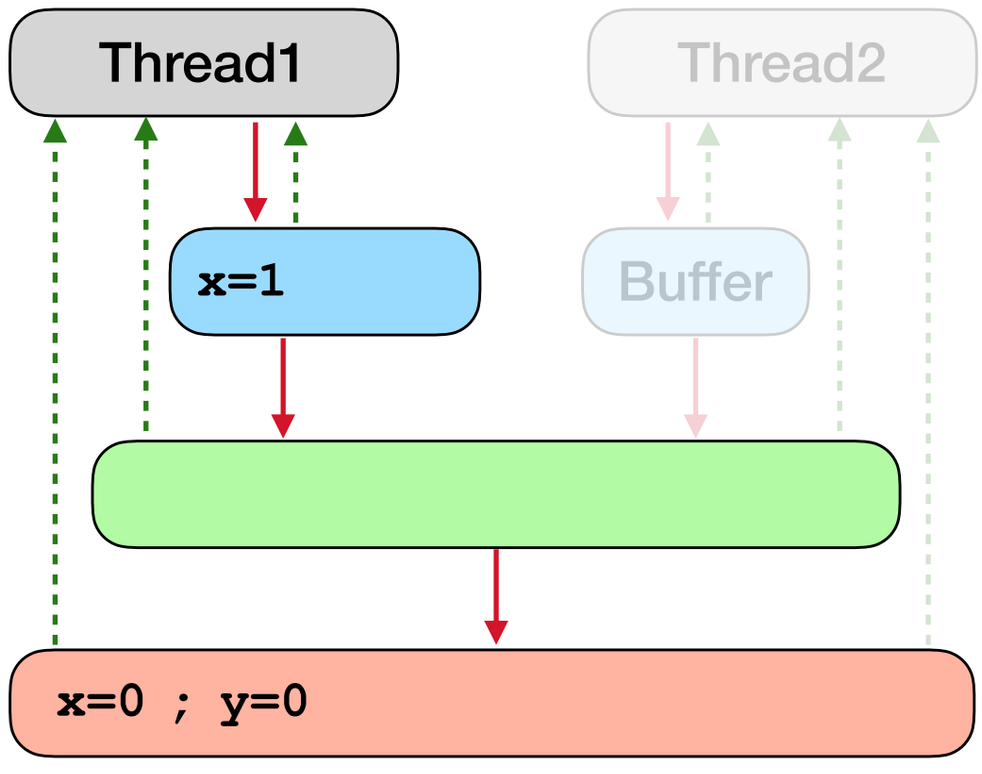

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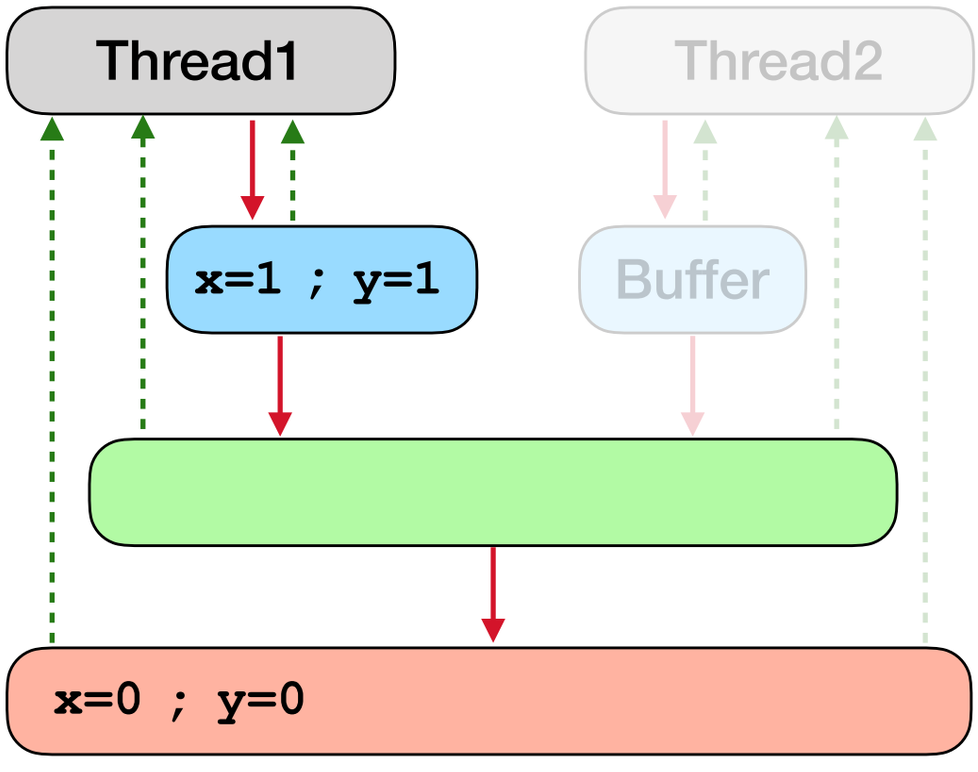

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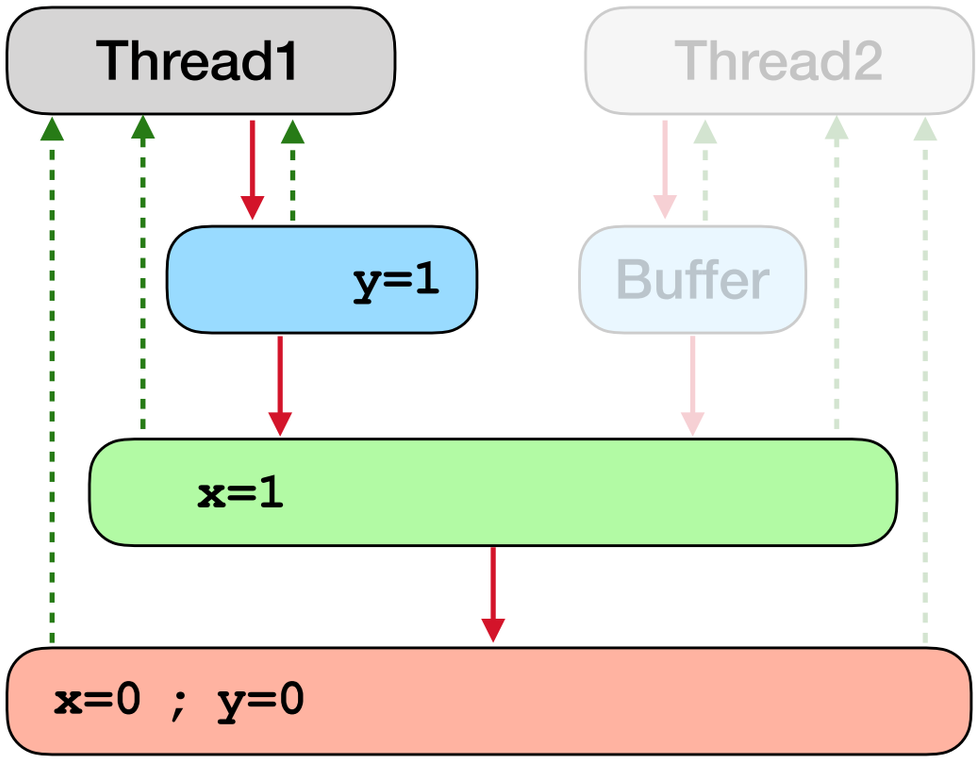

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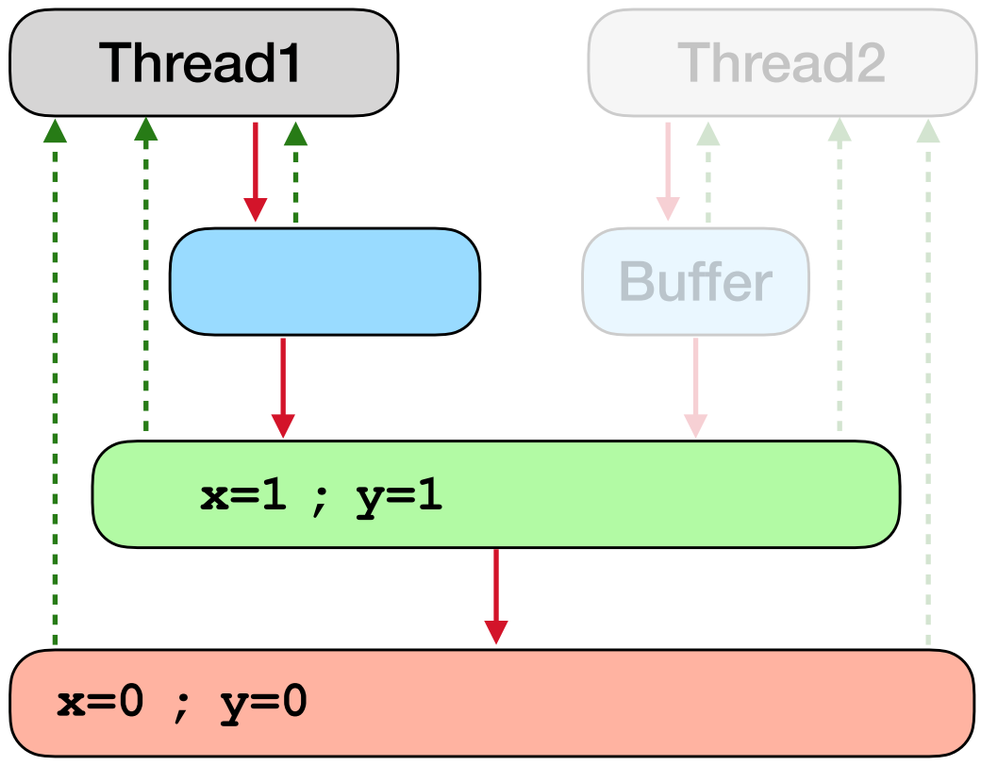

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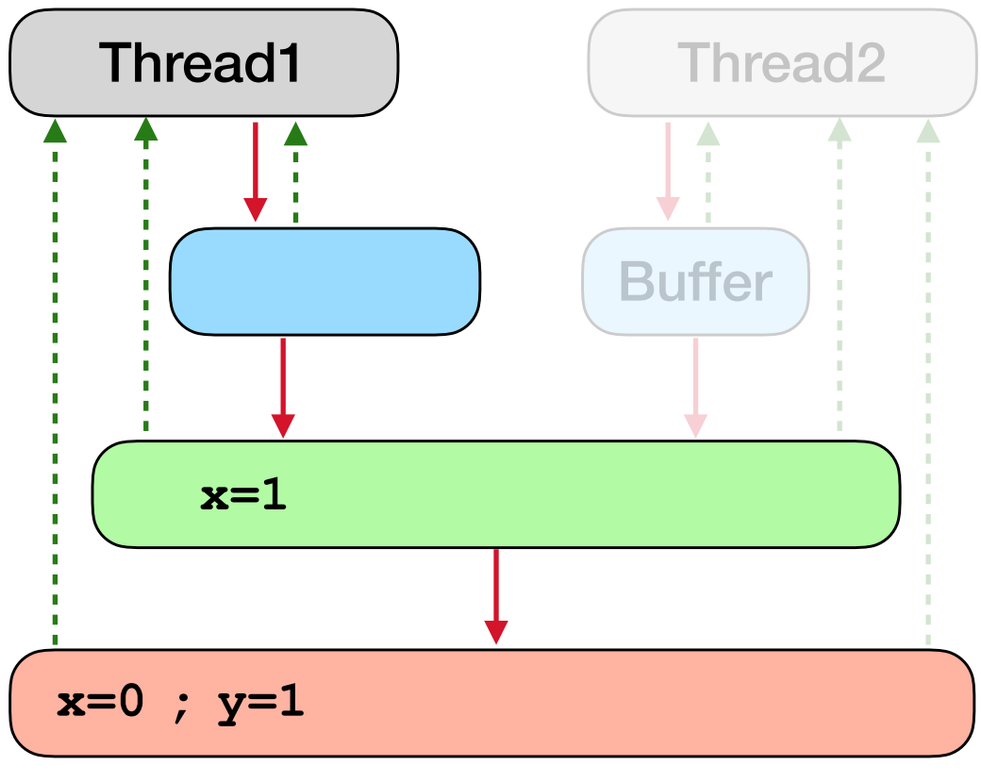

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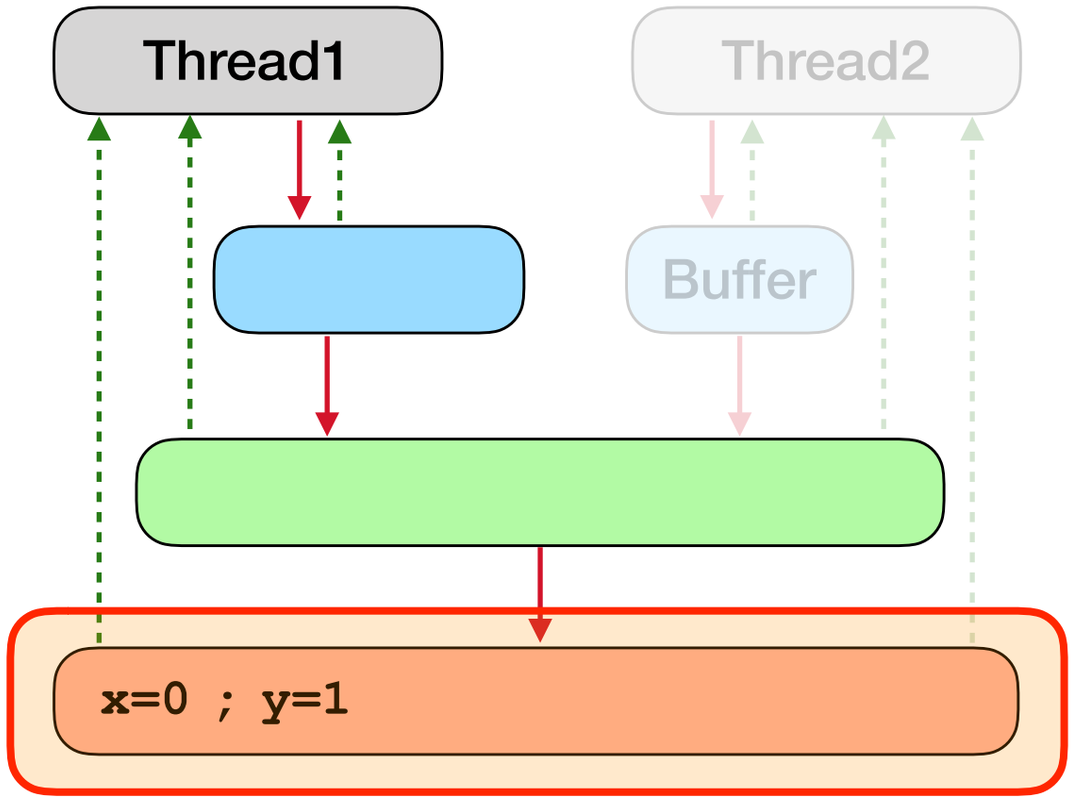

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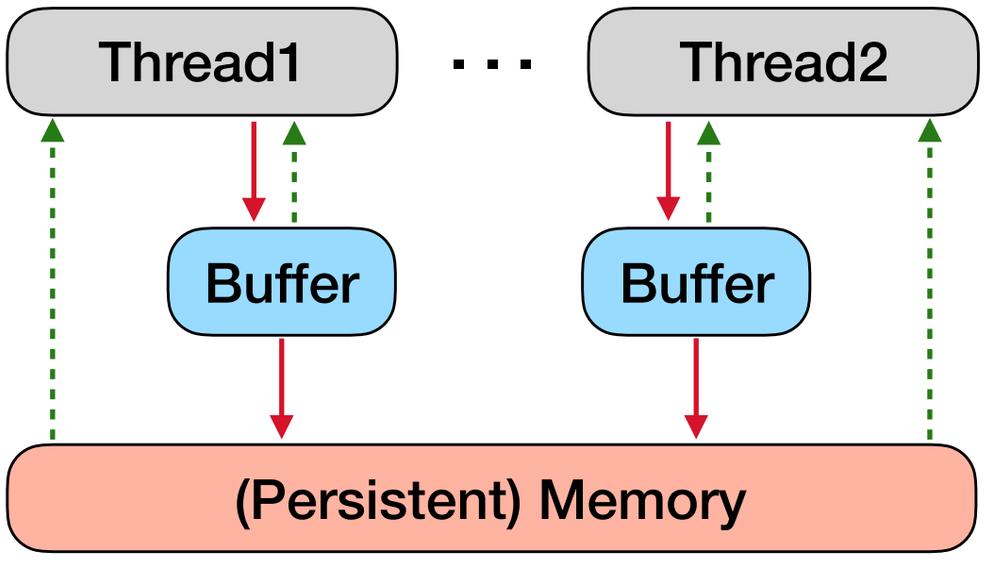

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// x=                                    y=1
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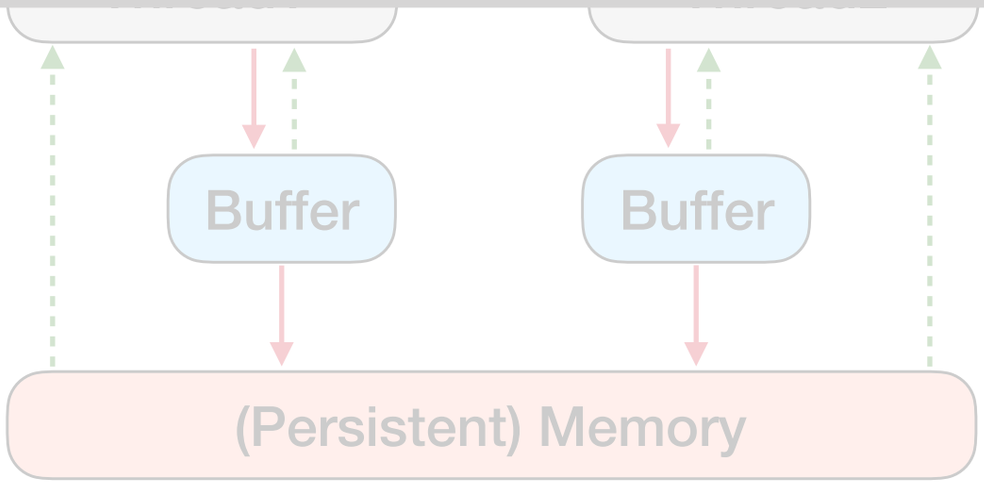
!! Write … *order*

How to model this when we ***remove the*** pbuffer?



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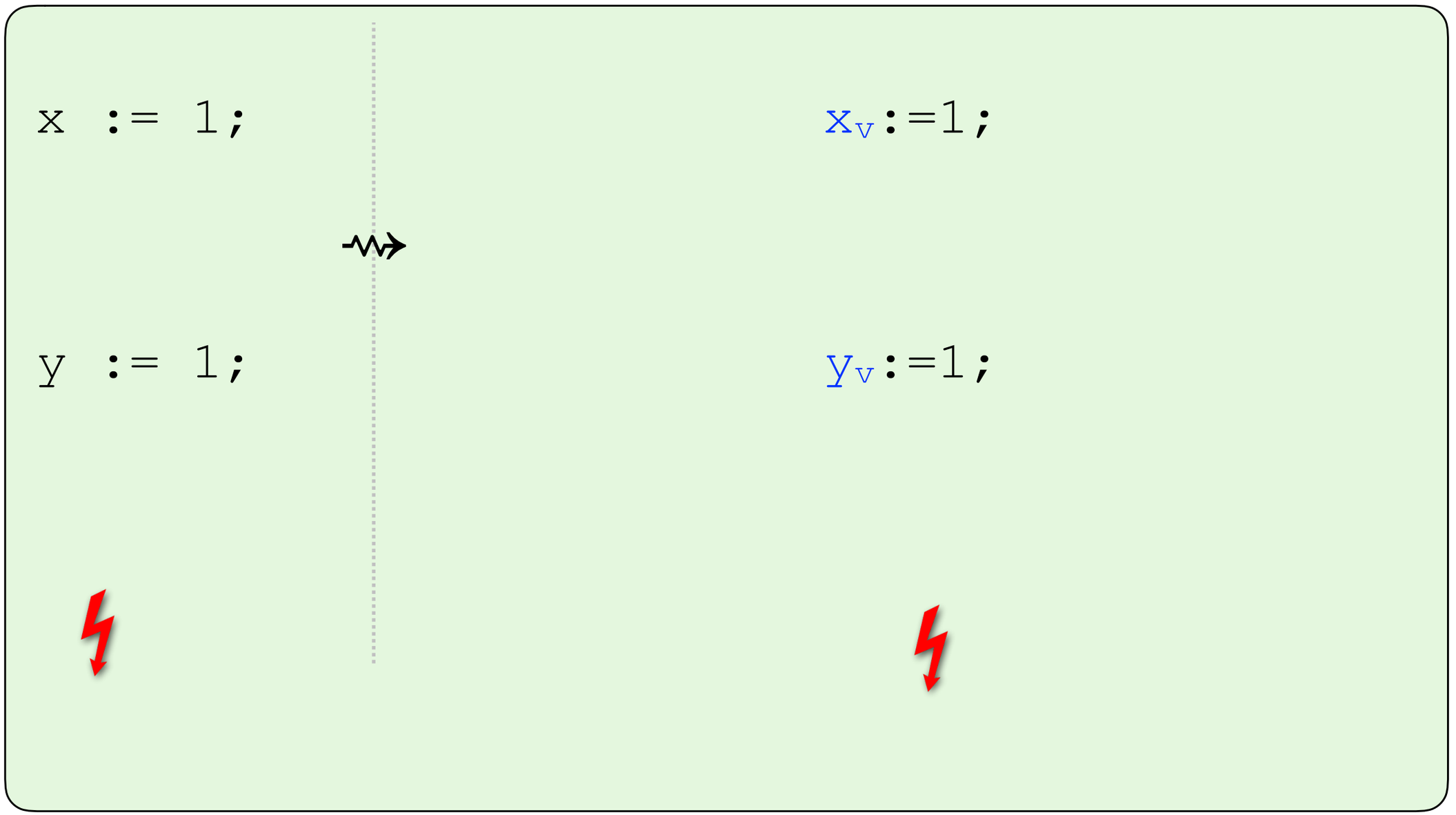


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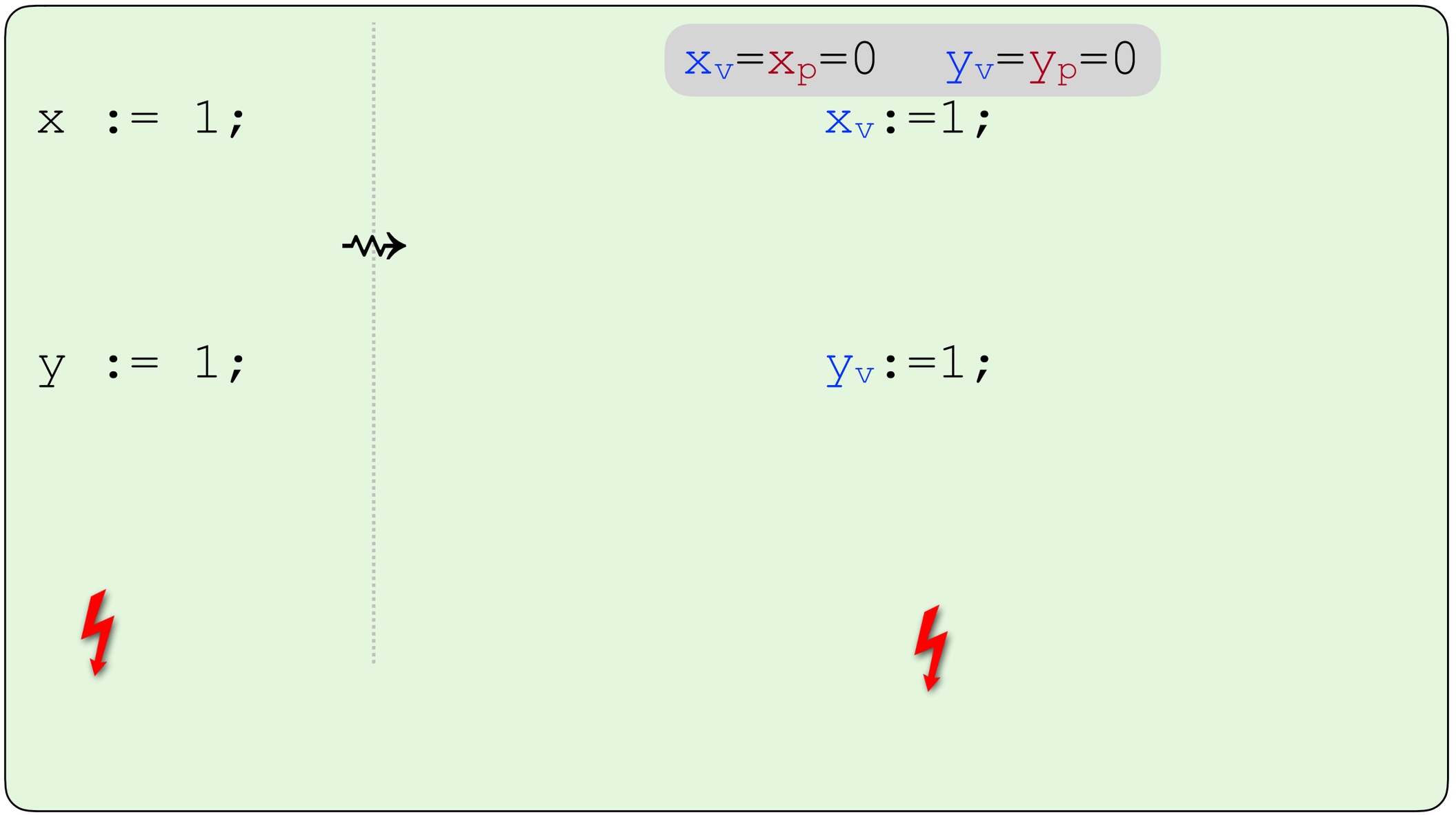


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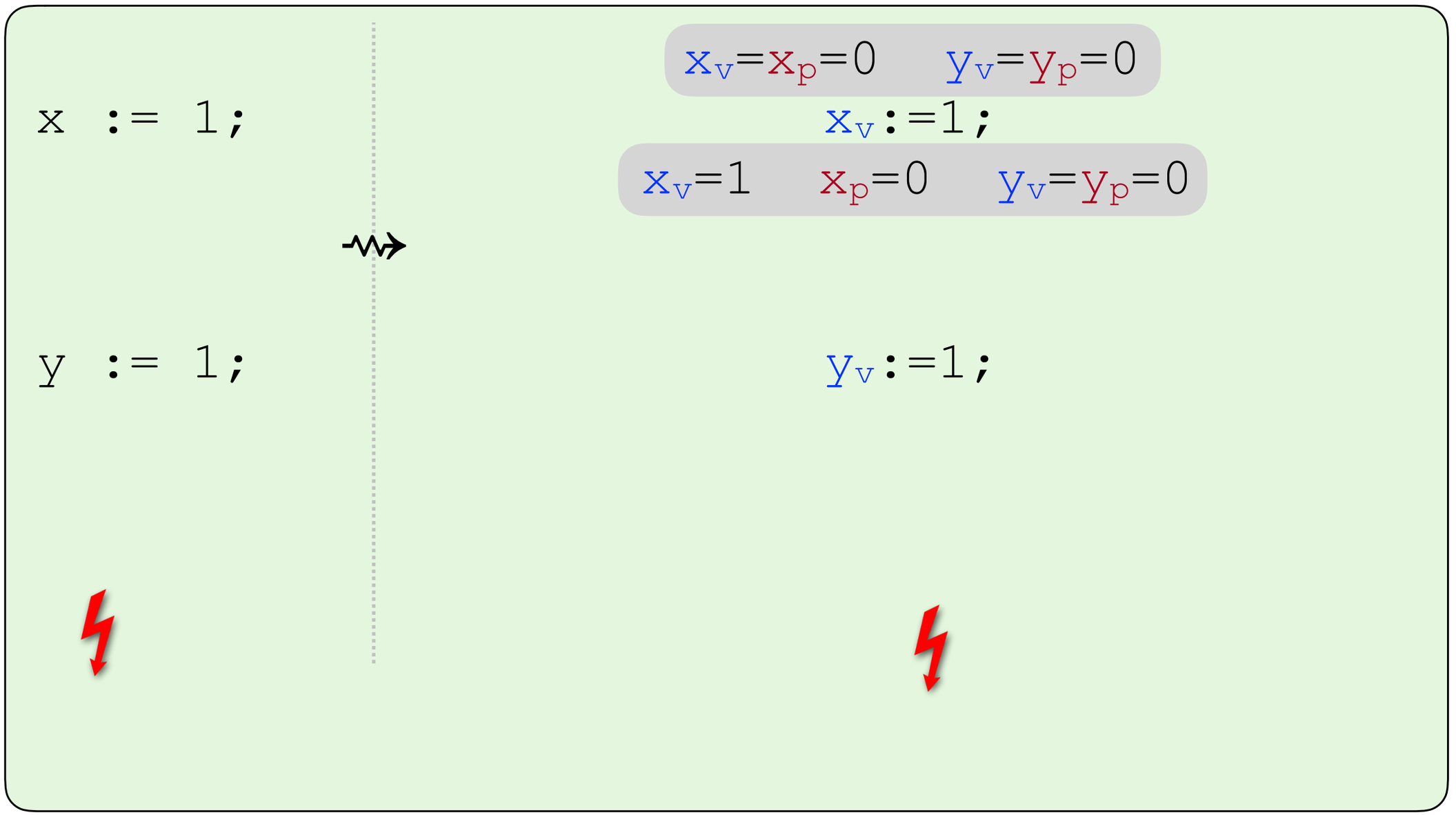


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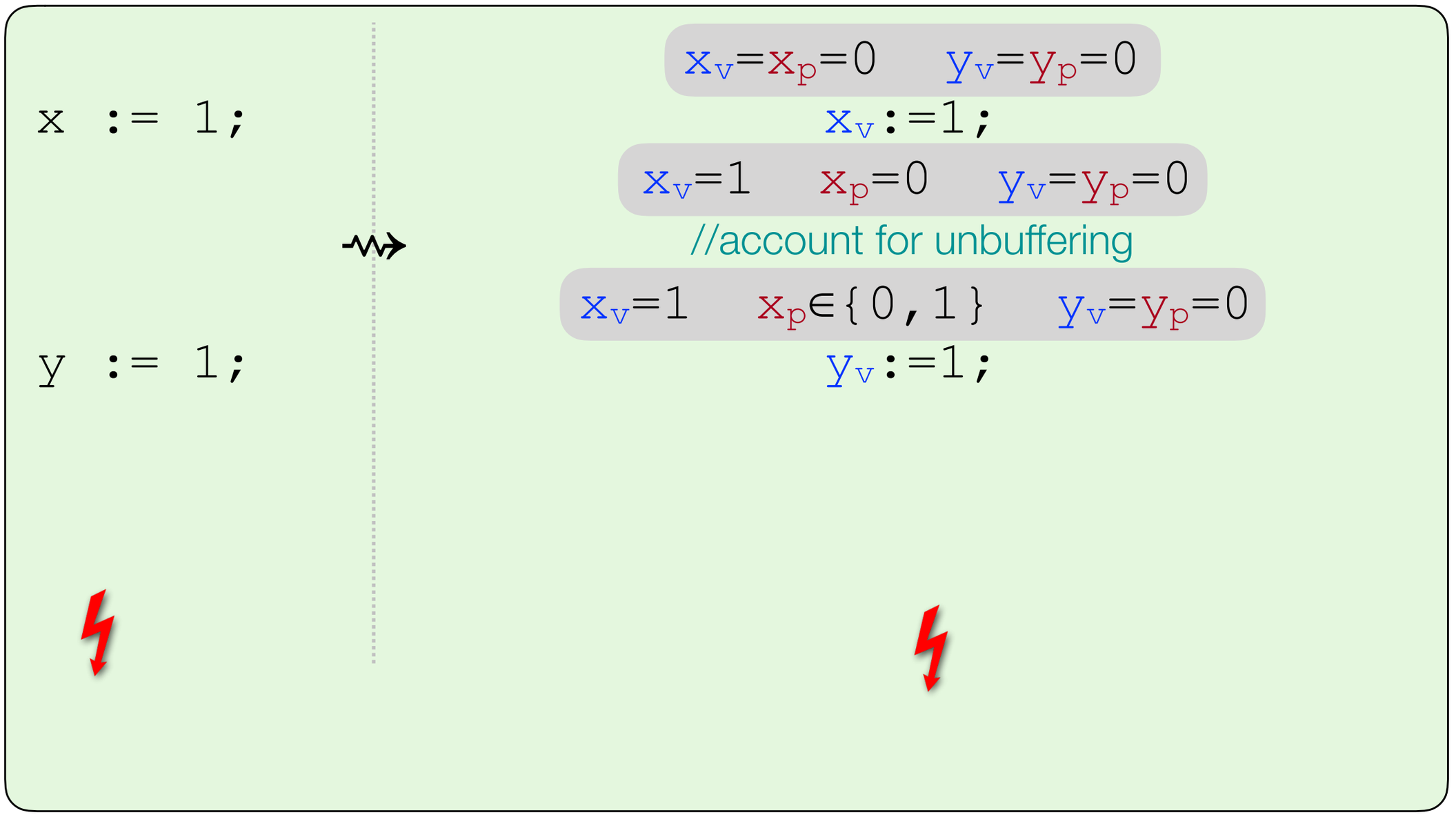


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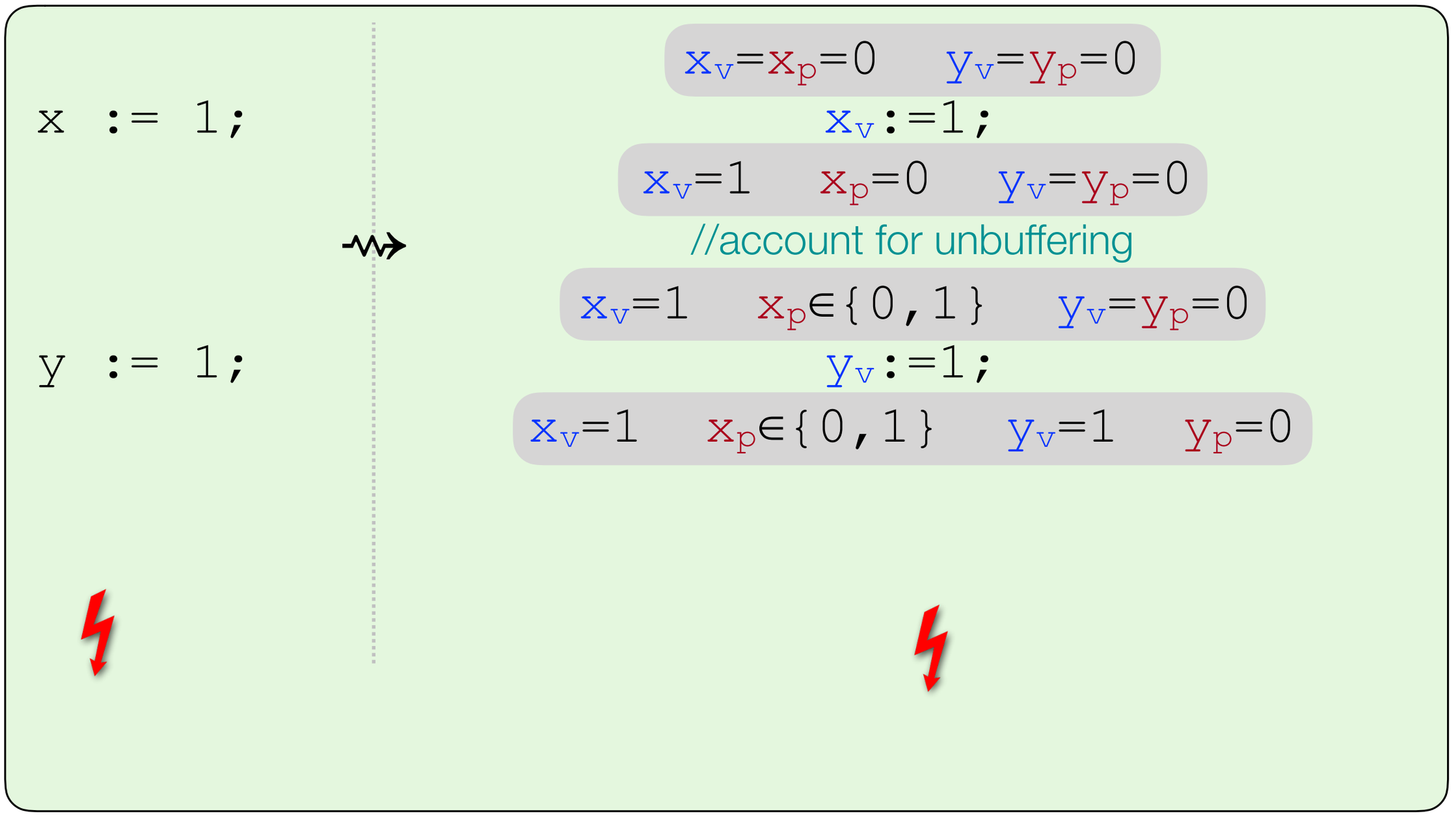


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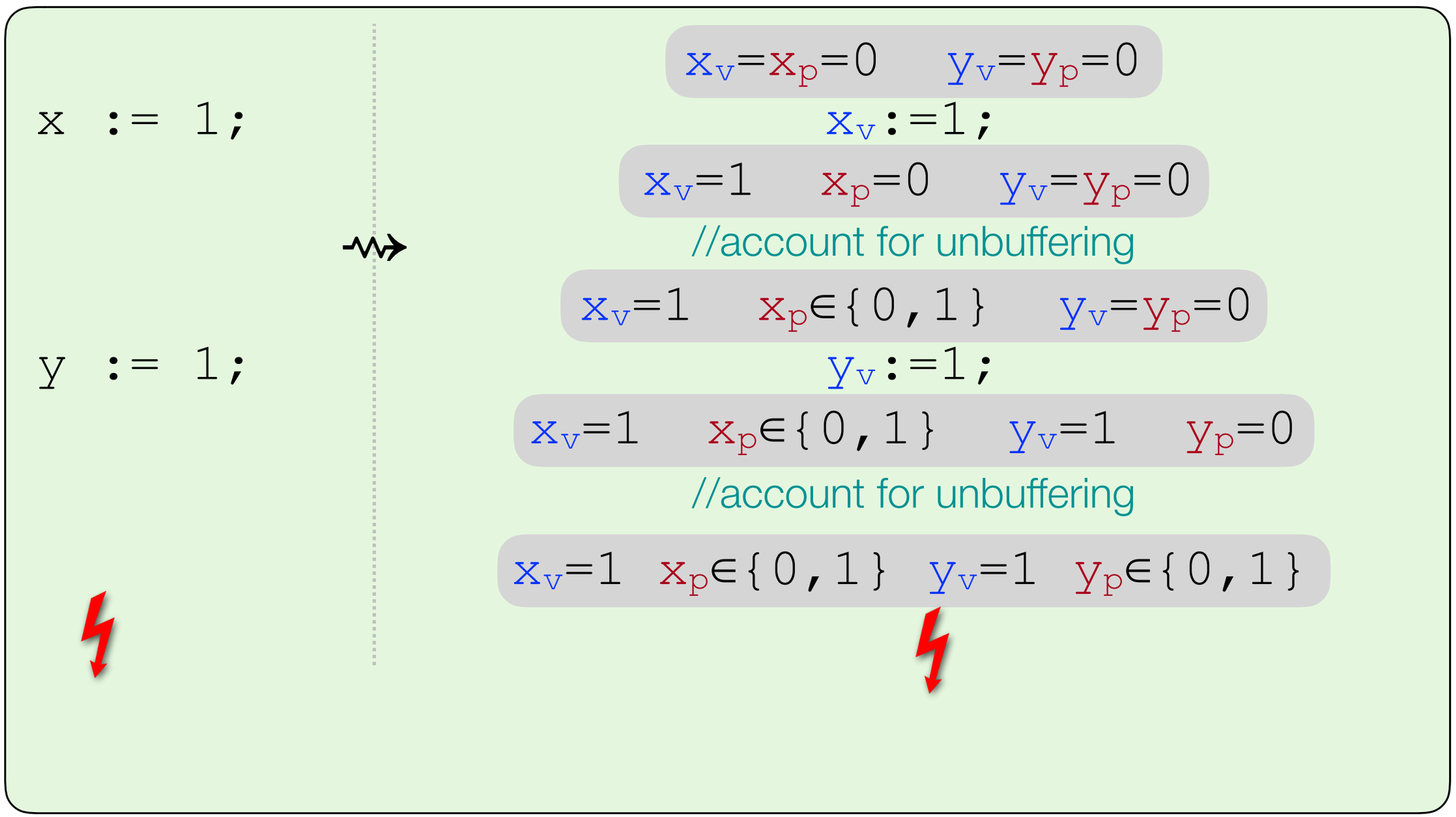


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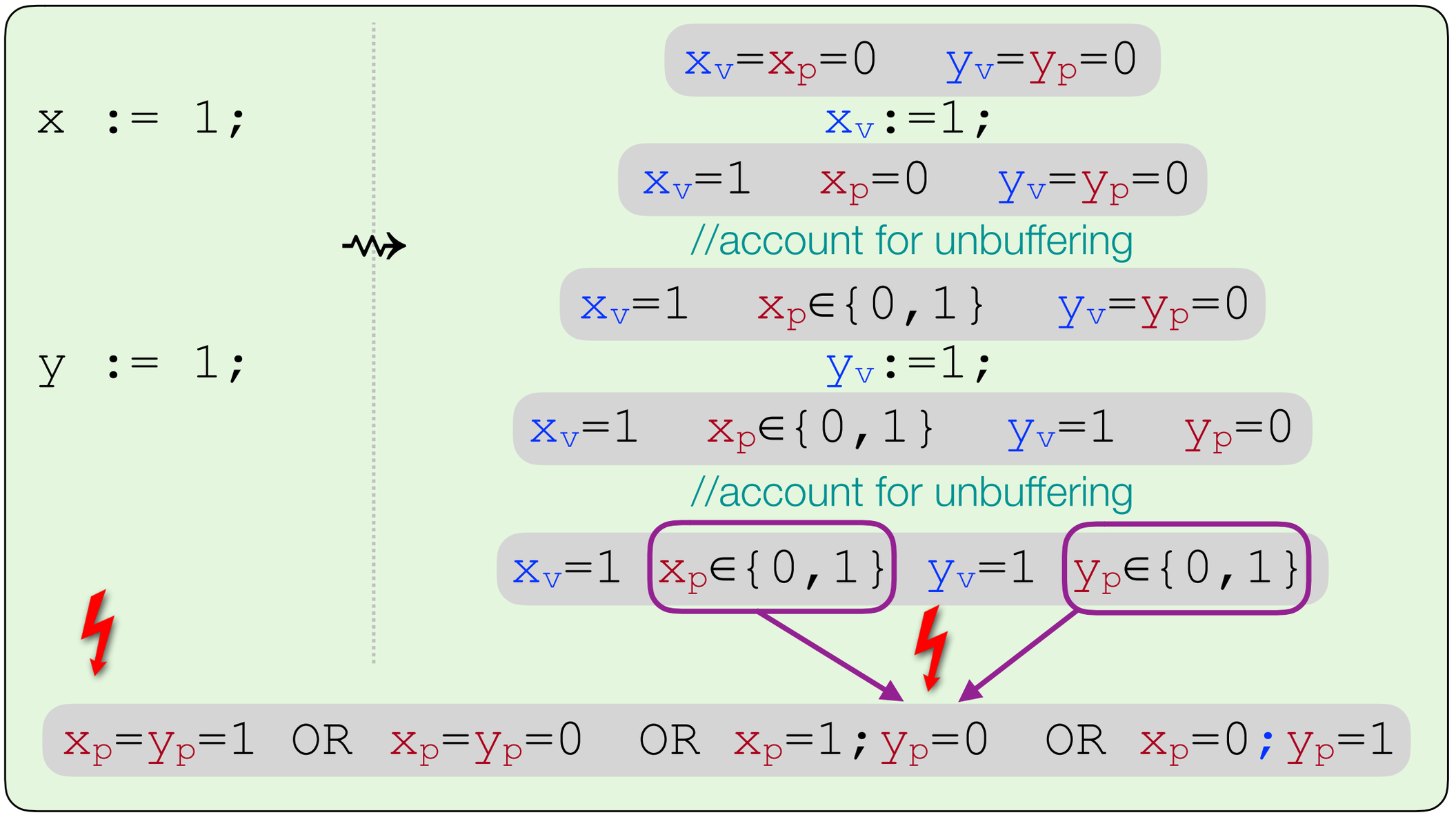


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| unbuffering (***non-det.*** times) | ⇝ | $x_p$:=$x_v$ |

# Challenge #2: ***Asynchronous Persists***

```
// x=y=0

    x := 1;
☛ flush x;
    y := 1;
```

# Challenge #2: ***Asynchronous Persists***

```
// x=y=0

    x := 1;
☛ flush x;
    y := 1;
```

```
// x=y=1   OR   x=y=0   OR   x=1;y=0   OR   x=0;y=1
```

!! Explicit persists order writes in pbuffer

# Challenge #2: ***Asynchronous Persists***

```
// x=y=0

    x := 1;
☛ flush x;
    y := 1;
```

```
// x=y=1   OR   x=y=0   OR   x=1;y=0   OR   x=0;y=1
```

!! Explicit persists order writes in pbuffer

!! Explicit persists behave ***asynchronously***

— flush `x` does evict writes on `x` from the pbuffer

# Challenge #2: ***Asynchronous Persists***

```
// x=y=0

x := 1;
flush x;
y := 1;
```

How to model this when we ***remove the*** pbuffer?

// x=y=1 OR x=1,y=0 OR x=0,y=1

!! Explicit persists order writes in pbuffer

!! Explicit persists behave ***asynchronously***

— flush x does evict writes on x from the pbuffer

# Ix86 and Asynchronous Persists — Naive Attempt

Record two versions per Location $x$:

$x_v$ : volatile version

$x_p$ : persistent version

***Px86-to-Ix86 Translation:***

| | | |
|---|---|---|
| $x := 1$ | ⇝ | $x_v := 1$ |
| $a := x$ | ⇝ | $a := x_v$ |
| unbuffering (***non-det.*** times) | ⇝ | $x_p := x_v$ |

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Record two versions per Location `x`:

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***Px86-to-Ix86 Translation:***

| | | |
|---|---|---|
| `x:=1` | ⇝ | $x_v$`:=1` |
| `a:=x` | ⇝ | `a:=`$x_v$ |
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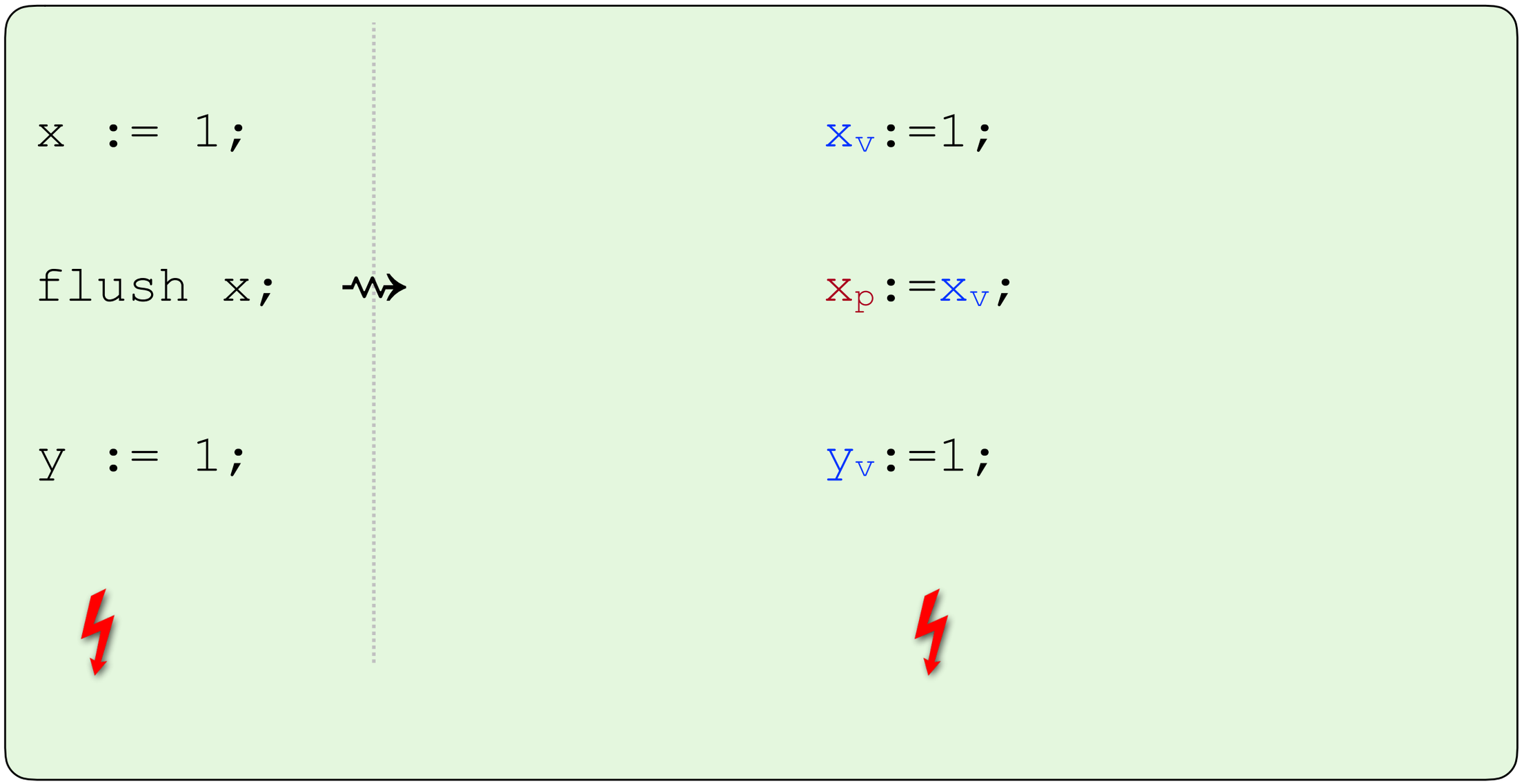


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|---|---|---|
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| a:=x | ⇝ | a:=$x_v$ |
| unbuffering (***non-det.*** times) | ⇝ | $x_p$:=$x_v$ |
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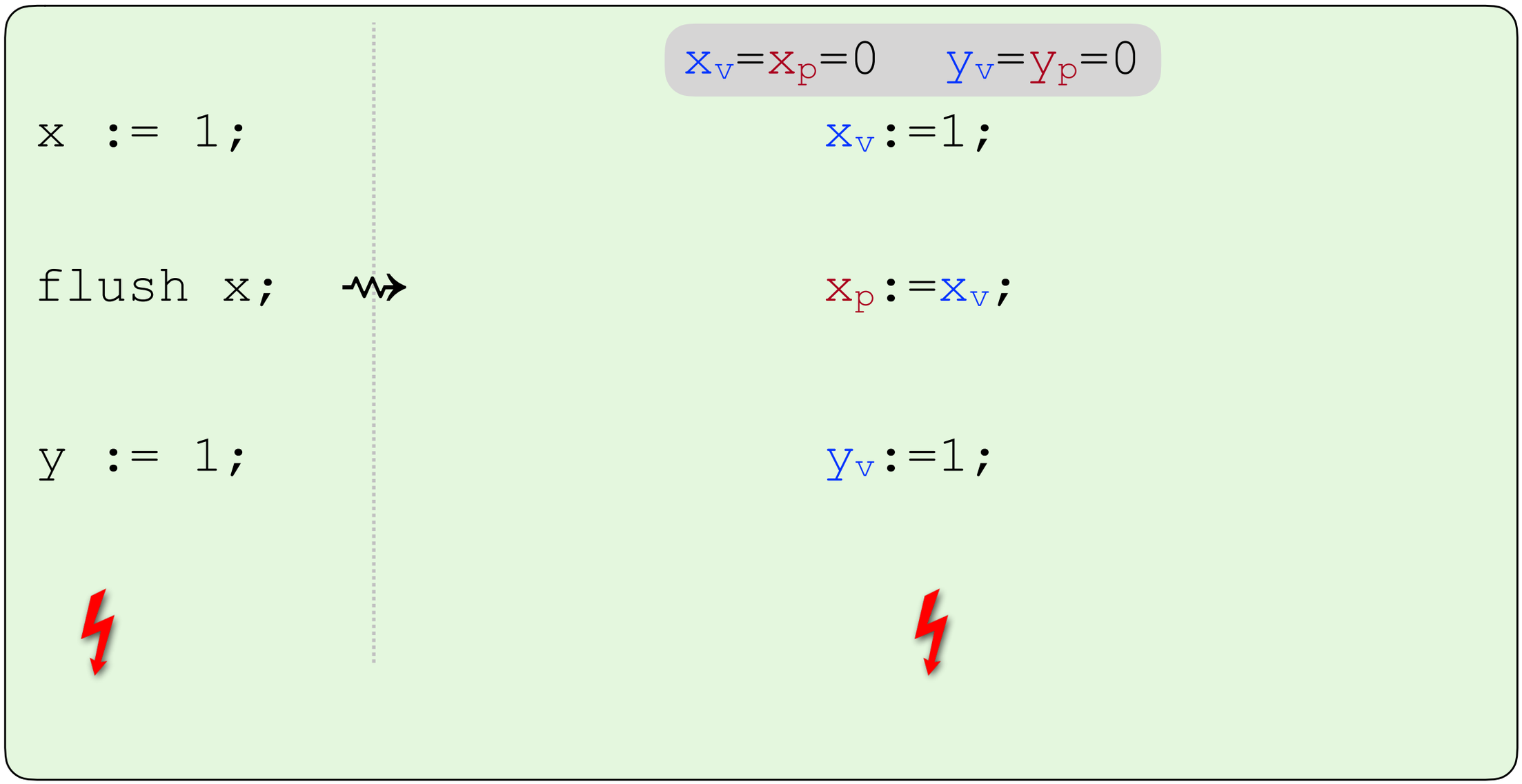


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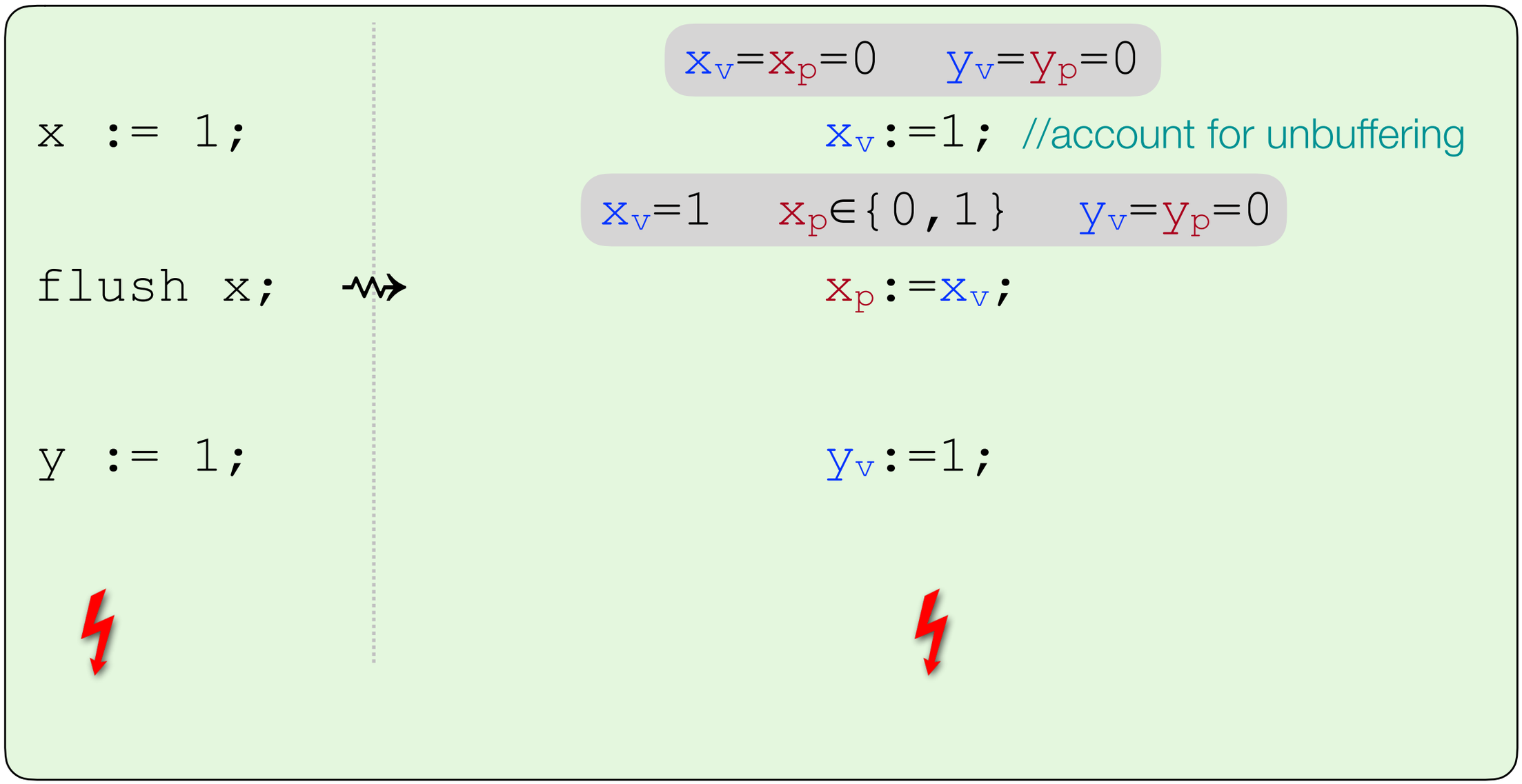


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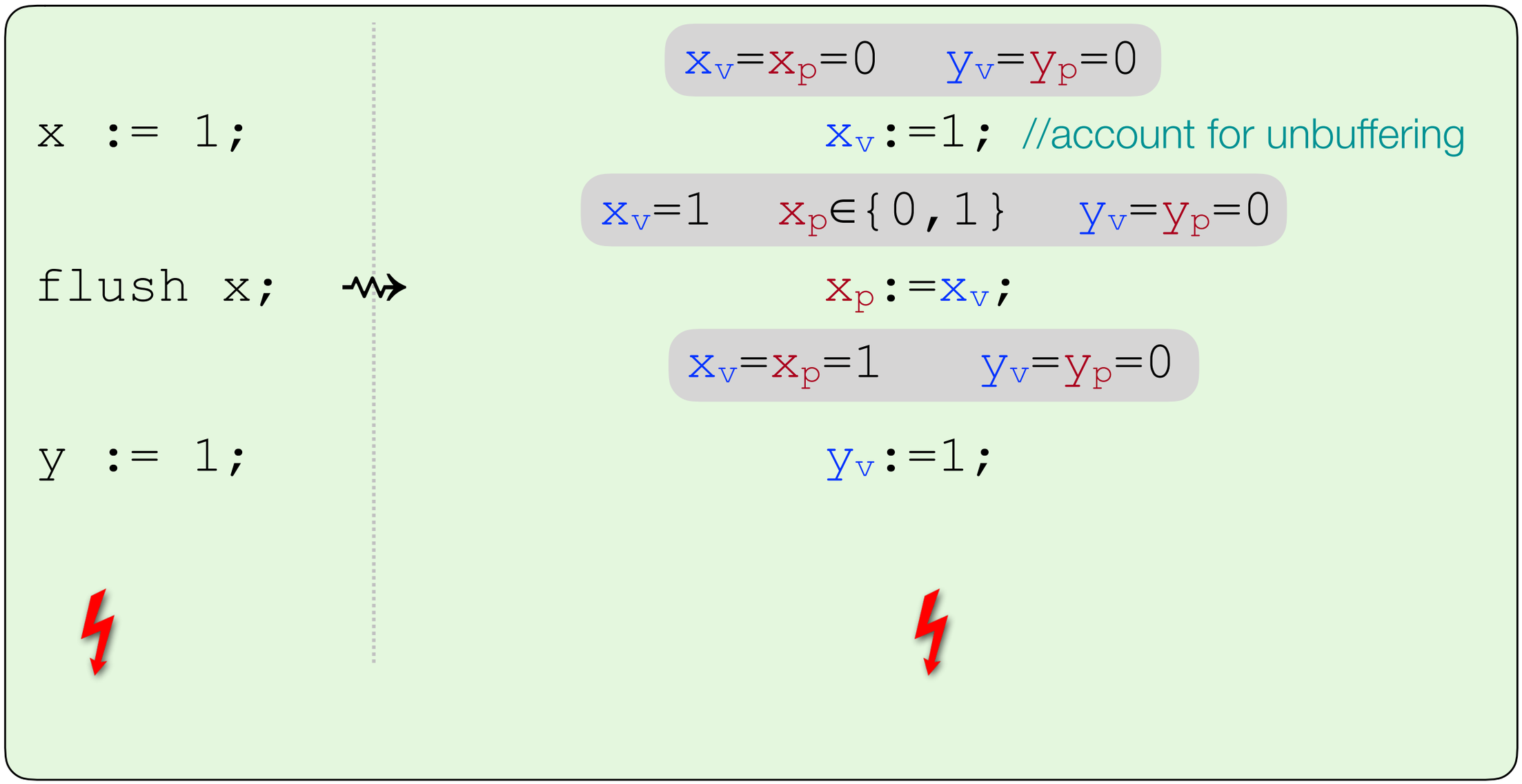


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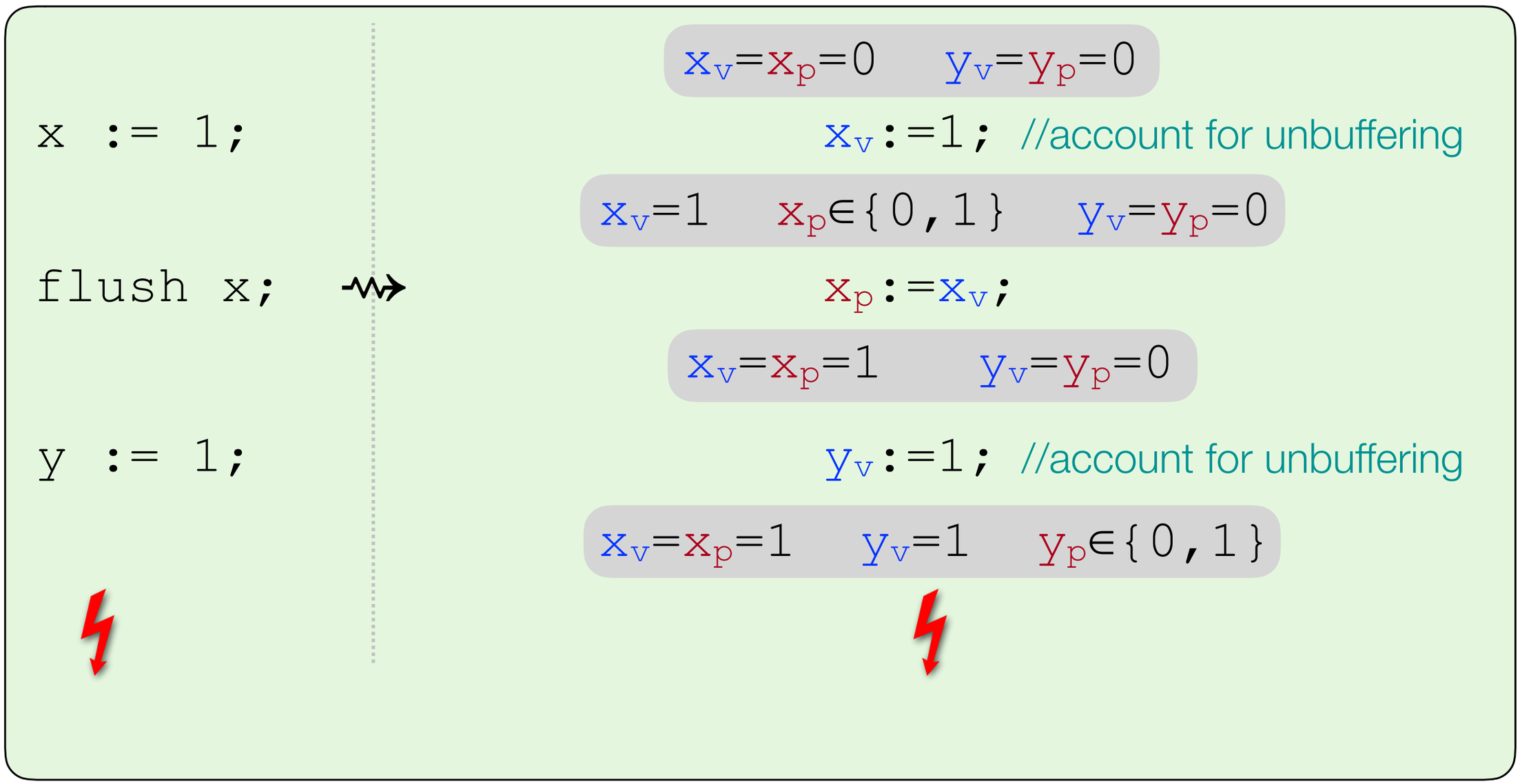


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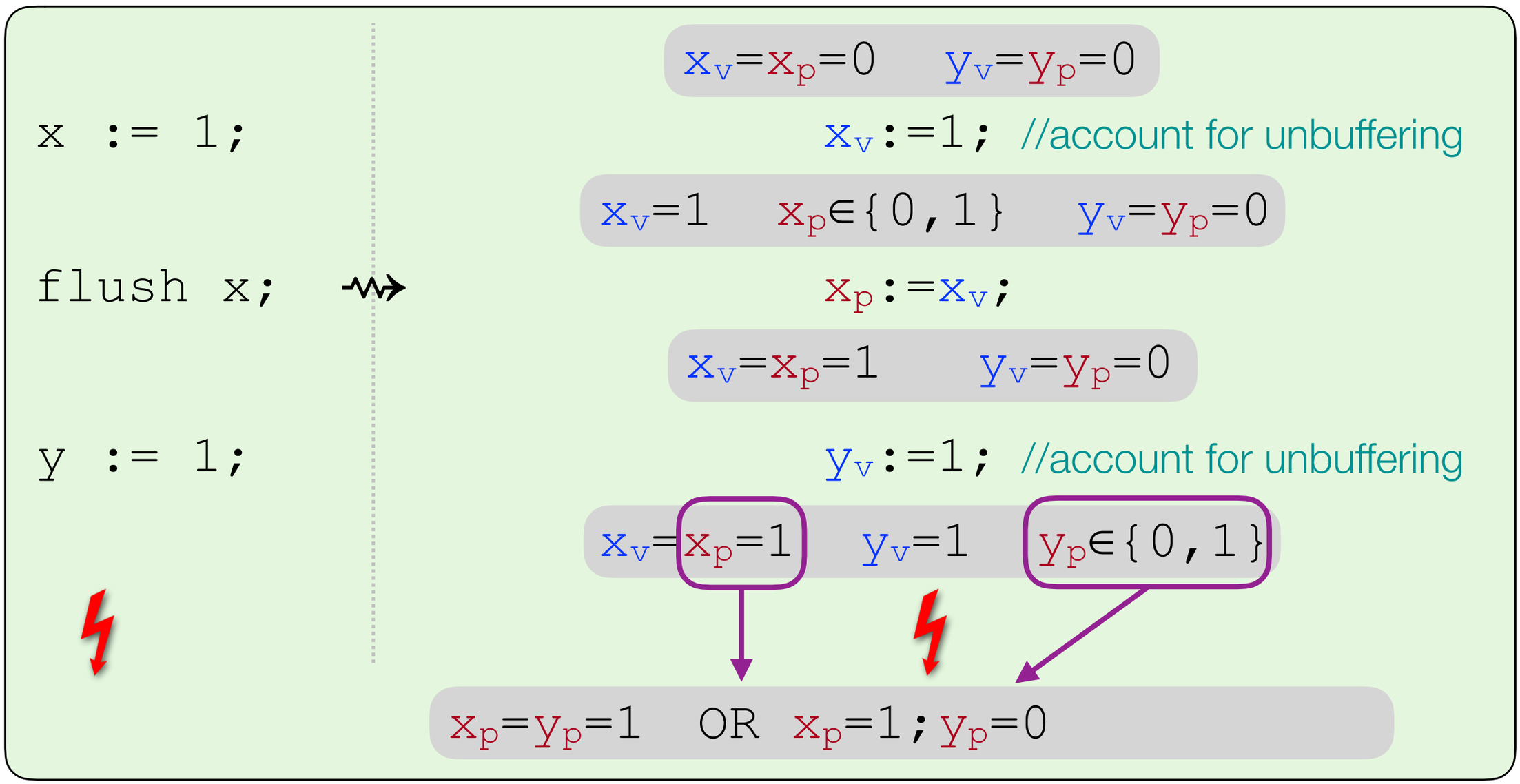


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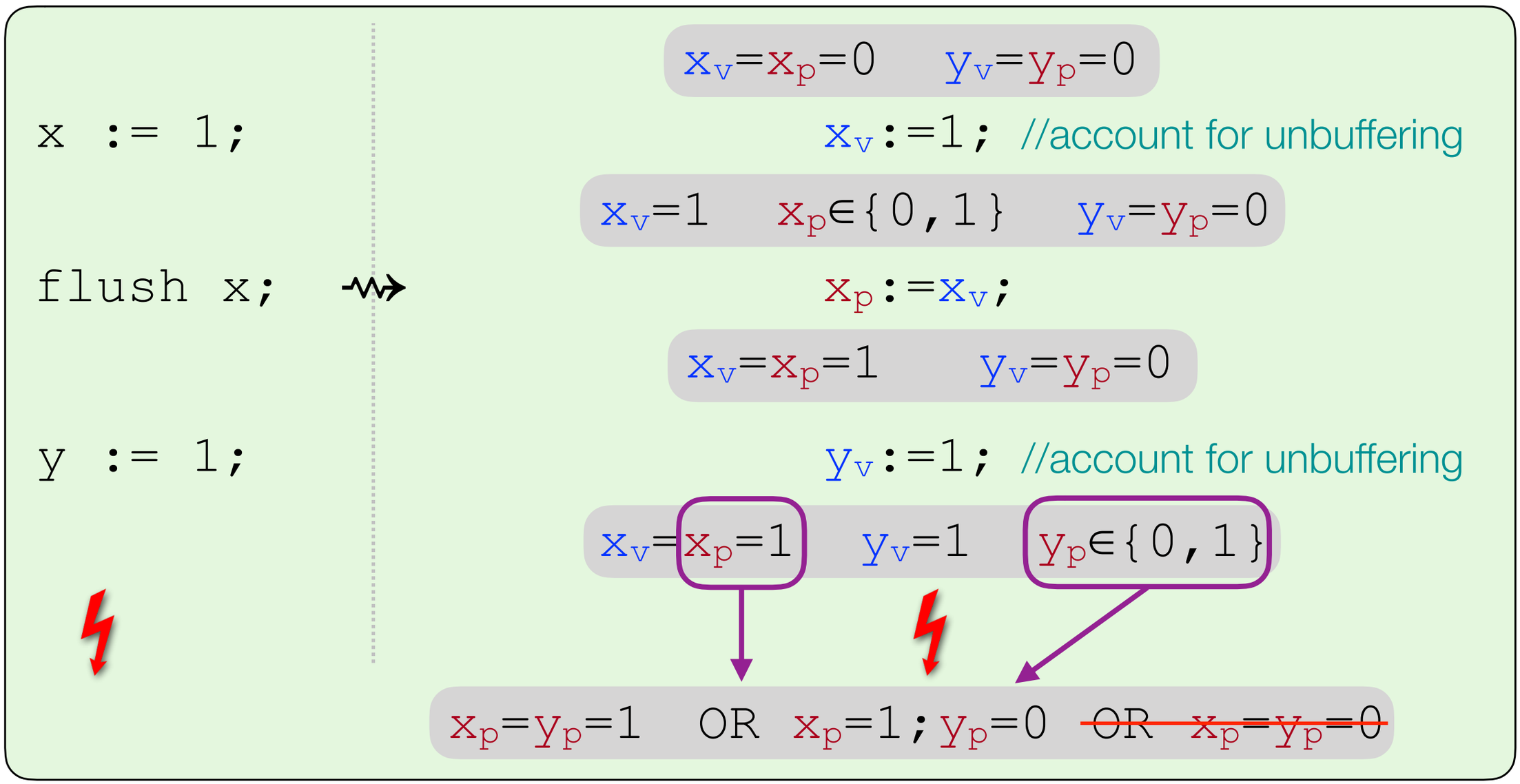


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| flush x | ⇝ | $x_p$:=$x_v$ |

# Ix86 and Asynchronous Persists — Naive Attempt

$x_v{=}x_p{=}0 \quad y_v{=}y_p{=}0$

`x := 1;` → $x_v{:=}1$; //account for unbuffering

$x_v{=}1 \quad x_p{\in}\{0,1\} \quad y_v{=}y_p{=}0$

`flush x;` ⇝ $x_p{:=}x_v$;

$x_v{=}x_p{=}1 \quad y_v{=}y_p{=}0$

`y :=` … buffering

**Problem**

Models `flush` ***synchronously***!

$x_p{=}y_p{=}1$ OR $x_p{=}1; y_p{=}0$ ~~OR $x_p{=}y_p{=}0$~~

| | | |
|---|---|---|
| `x:=1` | ⇝ | $x_v{:=}1$ |
| `a:=x` | ⇝ | $a{:=}x_v$ |
| unbuffering (***non-det.*** times) | ⇝ | $x_p{:=}x_v$ |
| `flush x` | ⇝ | $x_p{:=}x_v$ |

# Ix86 and Asynchronous Persists

Record ***three versions*** per Location `x`:

$x_v$ : volatile version

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$x_s$ : synchronous version
(for modelling `flush`)

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***Px86-to-Ix86 Translation:***

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| unbuffering (***non-det.*** times) (buffer→pbuffer) | ⇝ | $x_s$`:=`$x_v$ |

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Record ***three versions*** per Location `x`:

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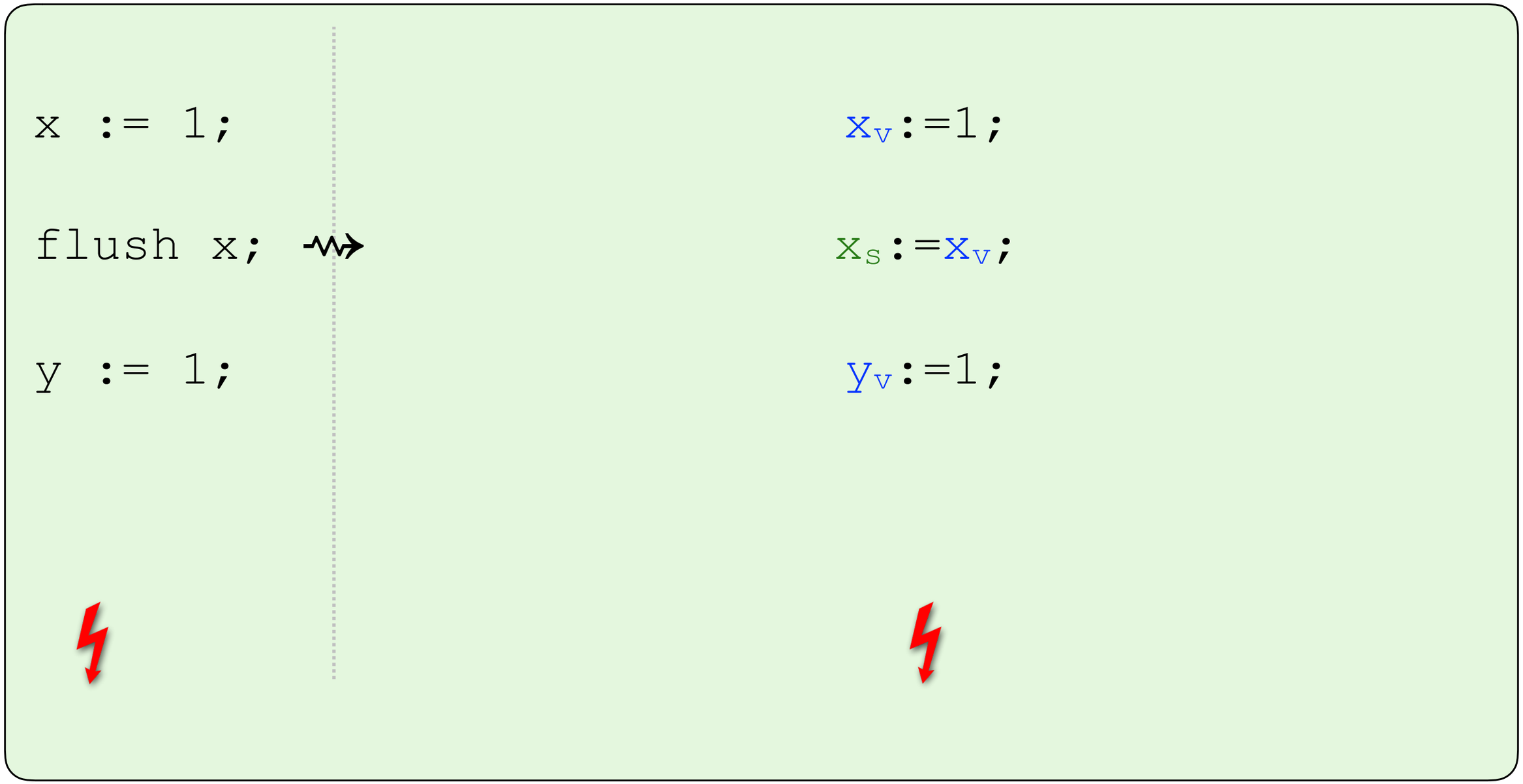


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# Ix86 and Asynchronous Persists

$x_v=x_s=x_p=0 \quad y_v=y_s=y_p=0$

| | |
|---|---|
| `x := 1;` | $x_v:=1;$ |
| `flush x;` ⇝ | $x_s:=x_v;$ |
| `y := 1;` | $y_v:=1;$ |

| | | |
|---|---|---|
| `x:=1` | ⇝ | $x_v:=1$ |
| `a:=x` | ⇝ | $a:=x_v$ |
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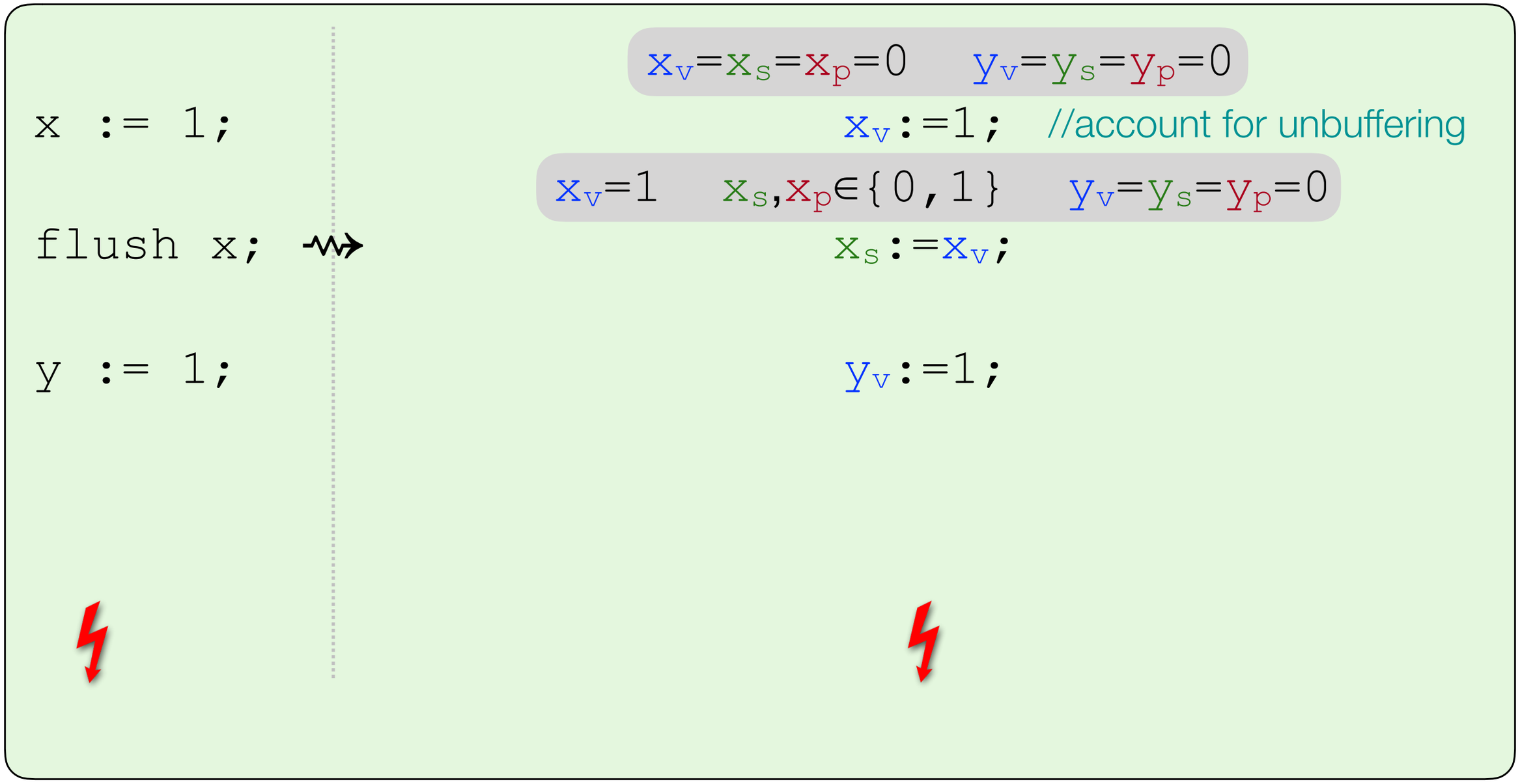


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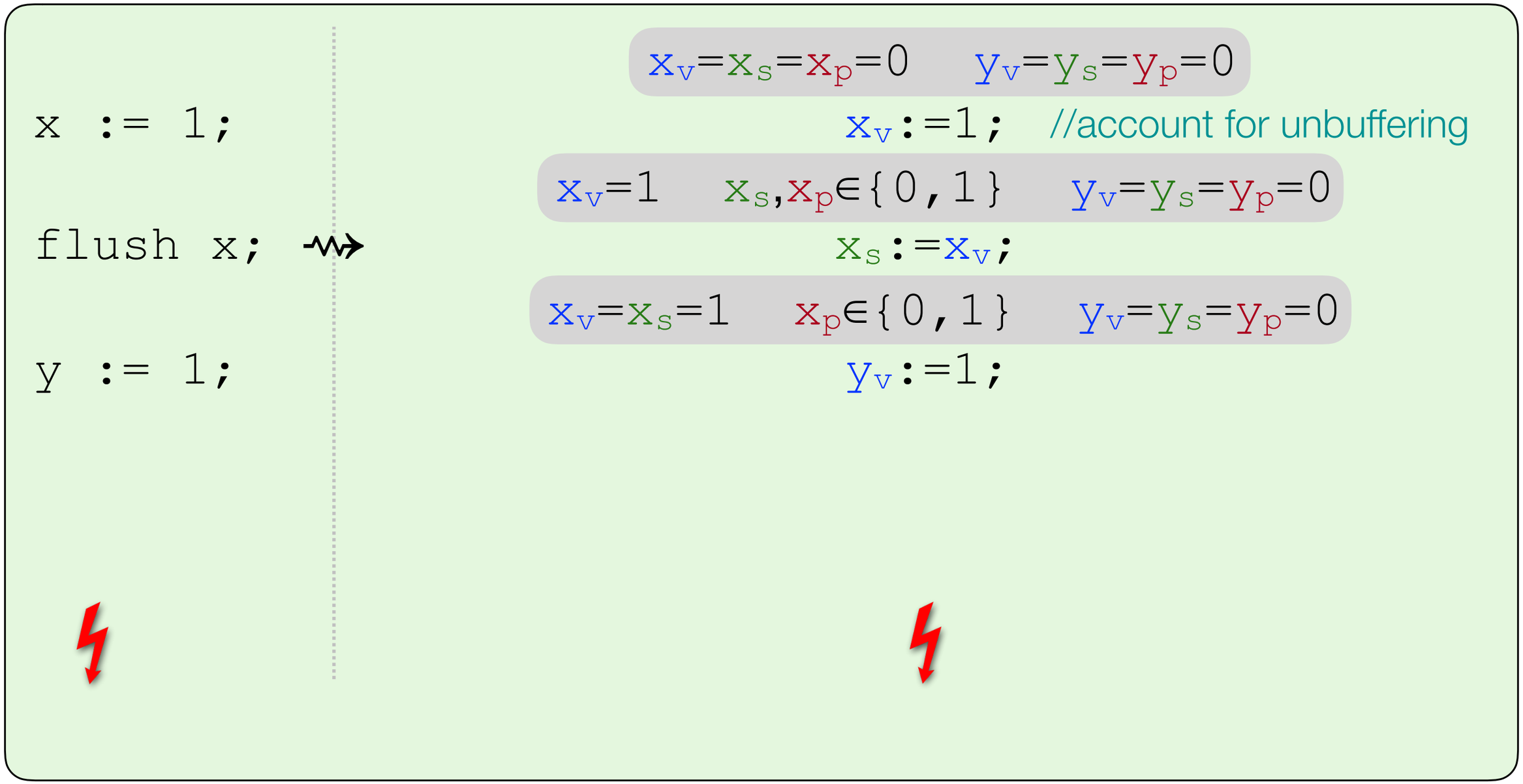


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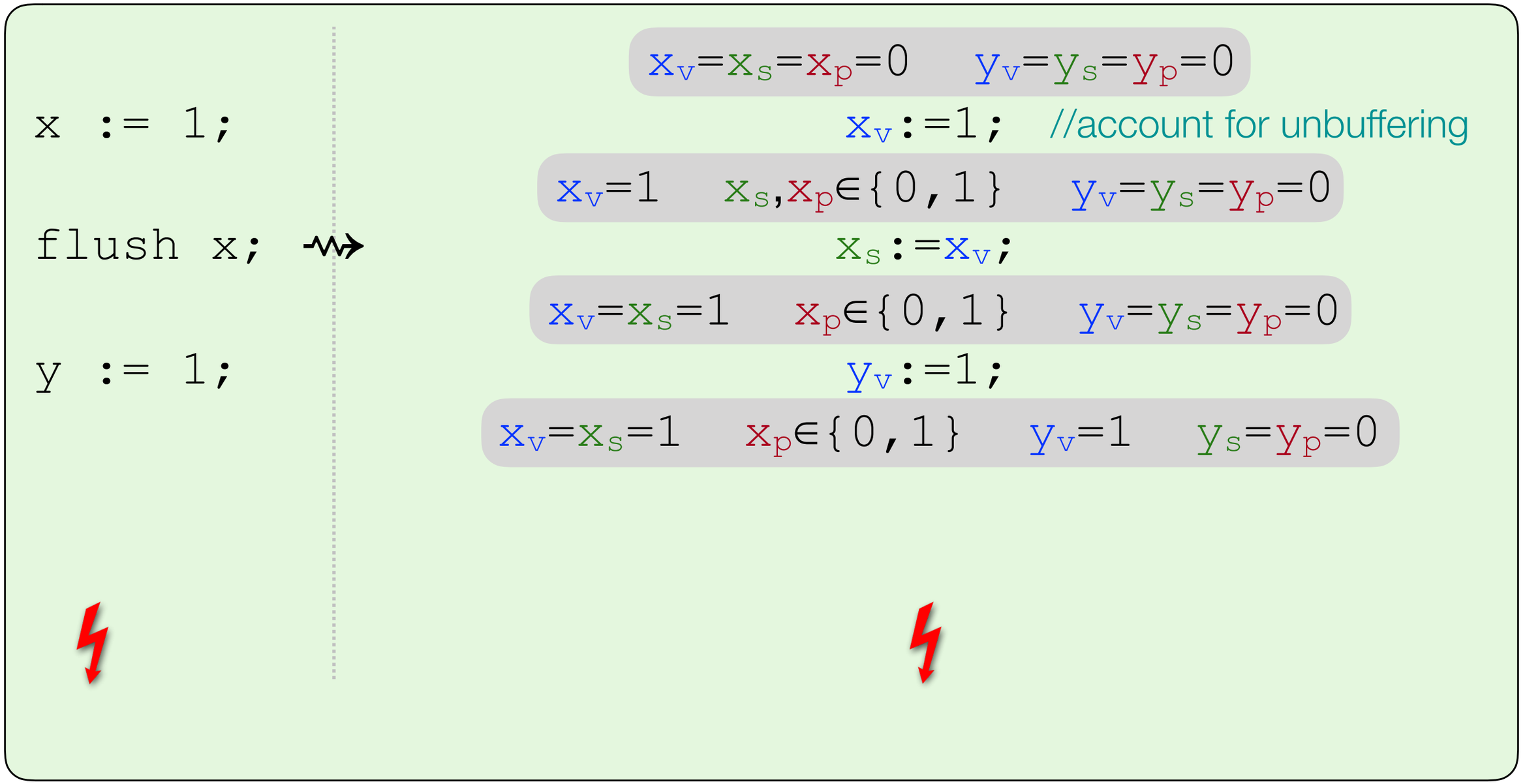


| | | |
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# Ix86 and Asynchronous Persists

```
x := 1;

flush x;  ⇝

y := 1;
```

$x_v{=}x_s{=}x_p{=}0 \quad y_v{=}y_s{=}y_p{=}0$

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$x_v{=}1 \quad x_s,x_p{\in}\{0,1\} \quad y_v{=}y_s{=}y_p{=}0$

$x_s{:=}x_v$;

$x_v{=}x_s{=}1 \quad x_p{\in}\{0,1\} \quad y_v{=}y_s{=}y_p{=}0$

$y_v{:=}1$;

$x_v{=}x_s{=}1 \quad x_p{\in}\{0,1\} \quad y_v{=}1 \quad y_s{=}y_p{=}0$

//account for unbuffering

$x_v{=}x_s{=}1 \quad x_p{\in}\{0,1\} \quad y_v{=}1 \quad y_s{\in}\{0,1\} \quad y_p{=}1{\Rightarrow}x_p{=}1$

| | | |
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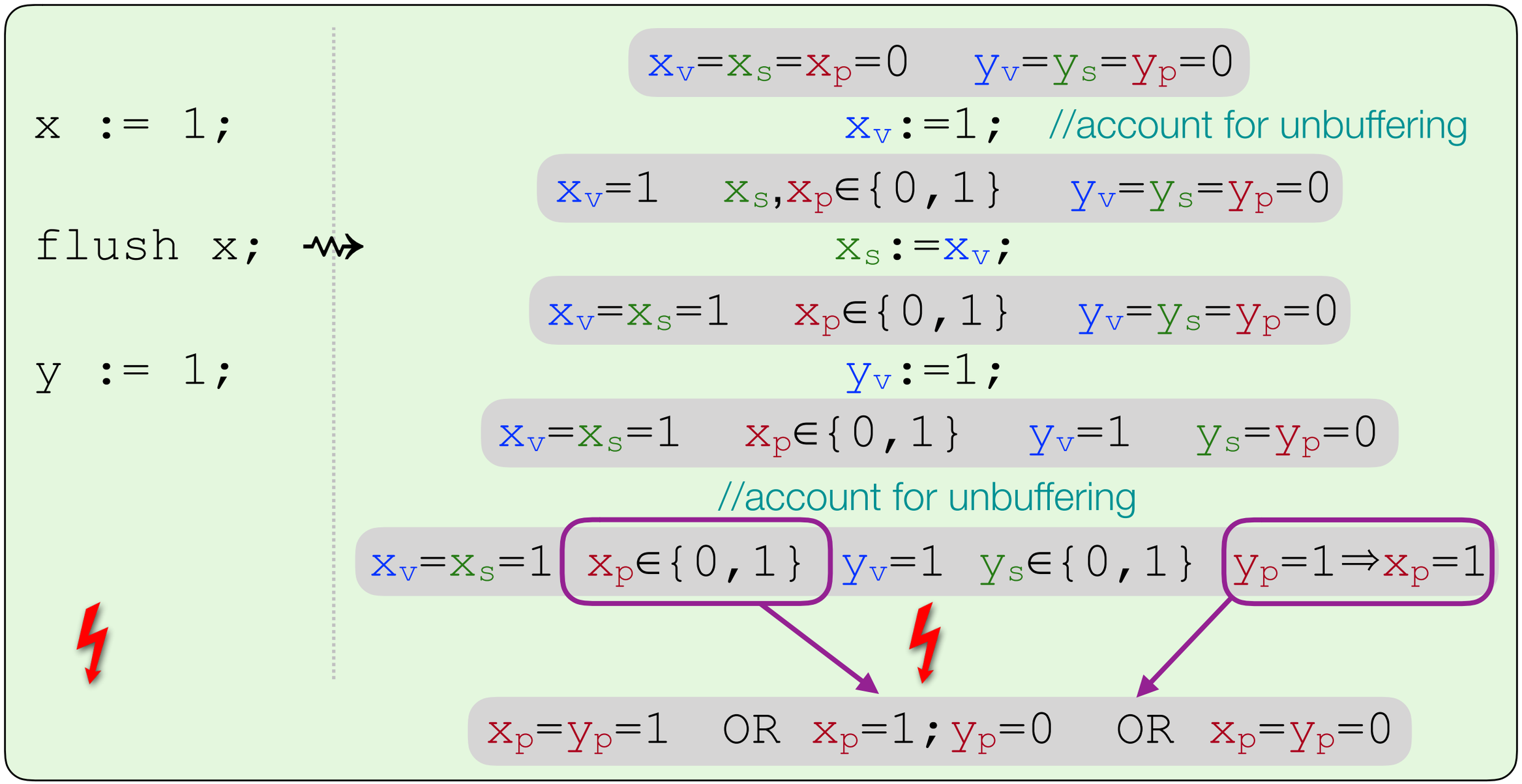


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# Challenge #3: ***Weak*** Asynchronous Persists

```
// x=y=0

x := 1;
☛ flushopt x;
y := 1;
```

```
// x=y=1   OR   x=y=0   OR   x=1;y=0
```

!! Weak explicit persists behave ***asynchronously***

# Challenge #3: ***Weak*** Asynchronous Persists

```
// x=y=0

x := 1;
y := 1;
☛ flushopt x;
```

```
// x=y=1   OR   x=y=0   OR   x=1;y=0
```

!! Weak explicit persists behave ***asynchronously***

!! Weak explicit persists may be ***reordered***

# Challenge #3: ***Weak*** Asynchronous Persists

```
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x := 1;
y := 1;
☛ flushopt x;
```

```
// x=y=1   OR   x=y=0   OR   x=1;y=0   OR   x=0;y=1
```

!! Weak explicit persists behave ***asynchronously***

!! Weak explicit persists may be ***reordered***

# Challenge #3: ***Weak*** Asynchronous Persists

```
// x=y=0
x := 1;
```

## ***Problem***

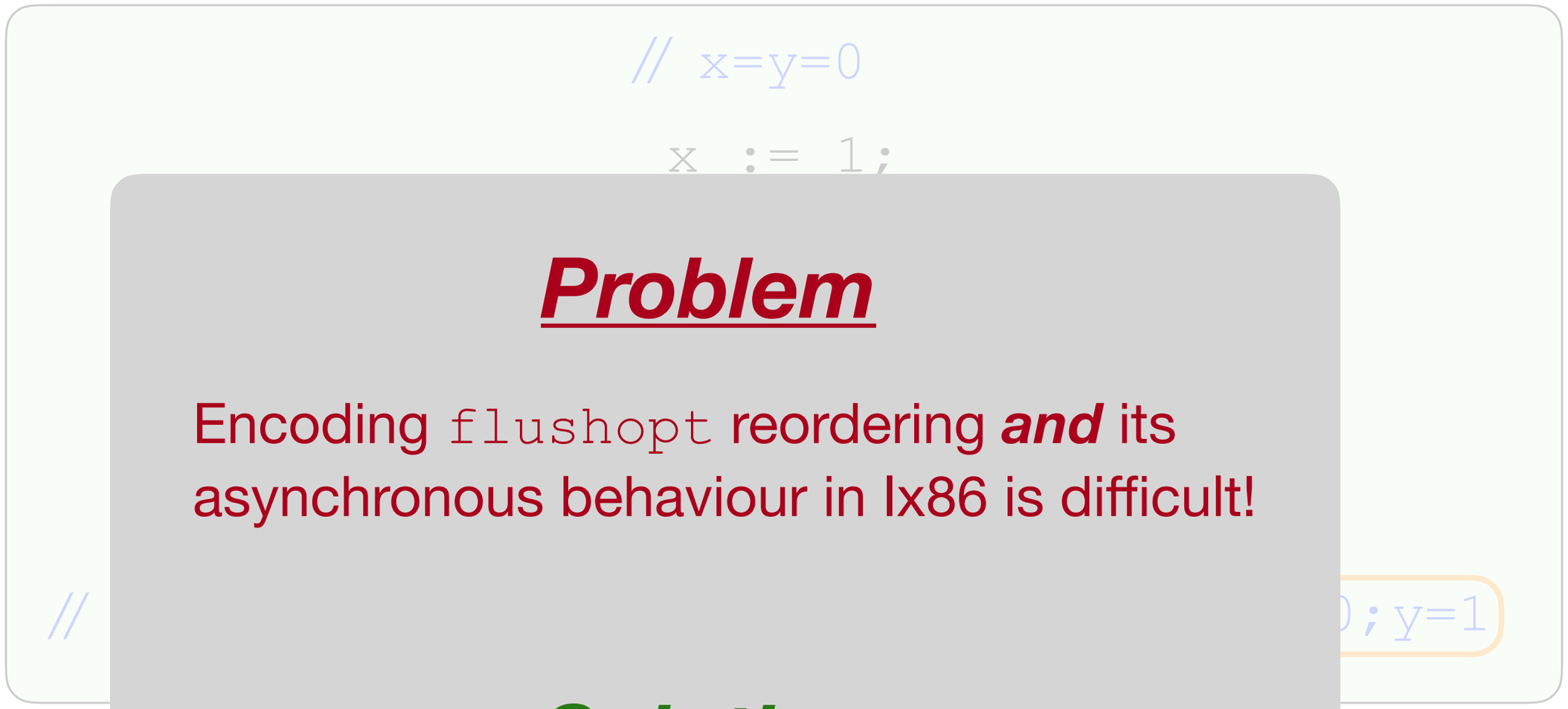
Encoding `flushopt` reordering ***and*** its asynchronous behaviour in Ix86 is difficult!

```
// 0;y=1
```

!! sly

!!

# Challenge #3: ***Weak*** Asynchronous Persists




## ***Problem***

Encoding `flushopt` reordering ***and*** its asynchronous behaviour in Ix86 is difficult!

## ***Solution***

Rewrite programs with `flushopt` to use `flush` instead!

# Eliminating `flushopt` Instructions

- **`flushopt`**
  - ➡ ***optimised*** variant of flush -- better performance
  - ➡ typically used in a particular ***programming pattern*** (epoch persistency)
  - ➡ ***transformation*** mechanism: rewrite programs with `flushopt`
    to ***equivalent*** ones with `flush`

# Conclusions

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- ***lx86***: instrumented x86 semantics
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  - ➡ ***translation*** from Px86 to lx86
  - ➡ addresses challenge #1 and challenge #2

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Px86 prog.
(with `flushopt`)

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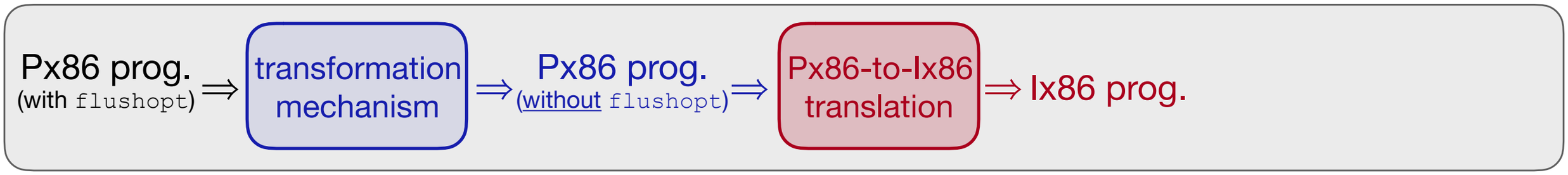

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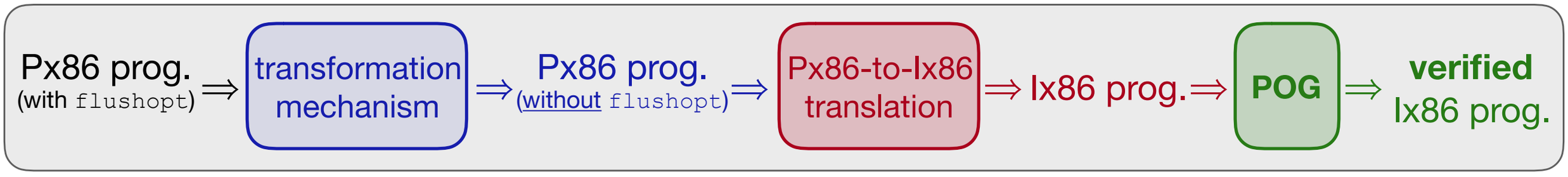

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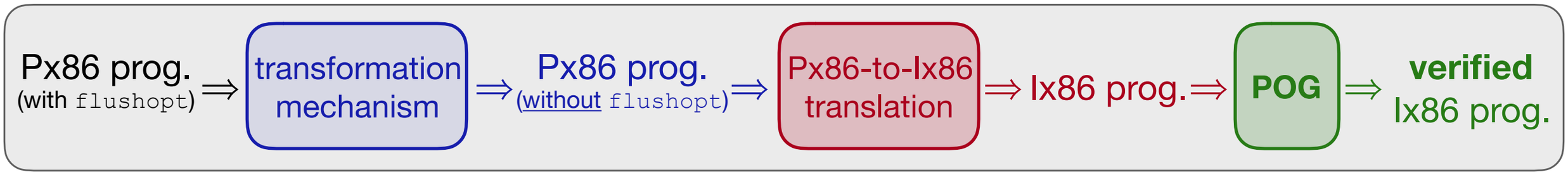


## Thank You for Listening!


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